CENTRE NATIONAL D'ÉTUDES SPATIALES

CNES feedback on the ATF280E FPGA and Space FPGA Designer

Workshop on fault-injection and fault-tolerance tools for reprogrammable FPGAs

ESTEC
11/09/2009

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Forecast :

► Background : final year internship « Comparative Evaluation of SEE Immune and reconfigurable FPGAs

► Part of the roadmap “ **reconfigurable payload** ” (MTRV)

► Comparaison of two SEE Immune and reconfigurable FPGAs :

vs

- The tools and the FPGAs
- From a " user point of view "

The two FPGAs :

Single Event Effects Immune Reconfigurable FPGAs

► The **ATF280E** from **Atmel Corp.** 	► **The " SIRF "** from **Xilinx** (**S**EU **I**mmune **R**econfigurable **F**PGA) 
- Not ITAR and European - Available (Engineering samples)	- ITAR and American - In development (avail : dec 2010)
• Same as AT40KEL040 (capacity x 7) → SEU hardened memory points. Available in QML-V	• " Hardened by design Virtex-5 VX130T " = No XTRM, no scrubbing.
• TOOLS : Synthesis : **Mentor Precision** Place & Route : **IDS Figaro**	• TOOLS : Synthesis (XST), place and route are integrated into one tool : **Xilinx ISE**

General features :

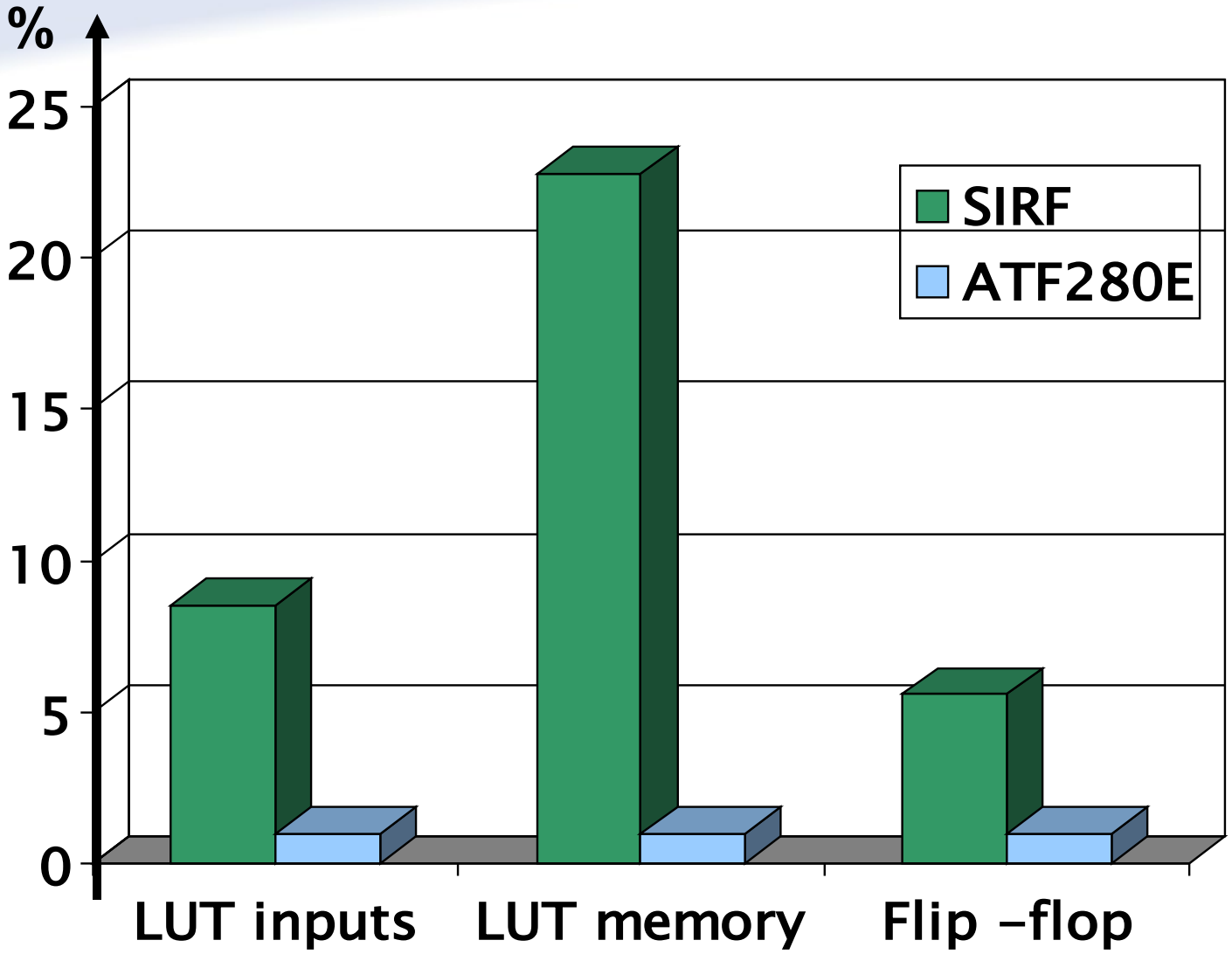
	ATF280E	SIRF
« ASIC Gates »	288K gates	“ 1,3 Million gates ”
Number of Core Cells / Slices	14 400 Core-Cells	20 480 Slices
User Ram	115,2 Kbit	10 728 Kbit
Clocks	8 Global and 4 Fast	32 Global networks
Maximum frequency	100 MHz internal, 50 MHz system	550 MHz internal, 250 MHz system
Cores voltages	1,8 V	1,0 V
Packages	MCGA 472	CF1144
User I/O	308 max + LVDS I/Os	com version. : 840 Single Ended Pins
Standards I/O	CMOS, TTL 1,8/3,3V, No 5 V Tolerance 8 LVDS Receiver/Tranceiver	≈ 25 standards (1,2V / 1,5V / 1,8V / 3,3V)
Die size	225 mm^2	146 mm^2

+

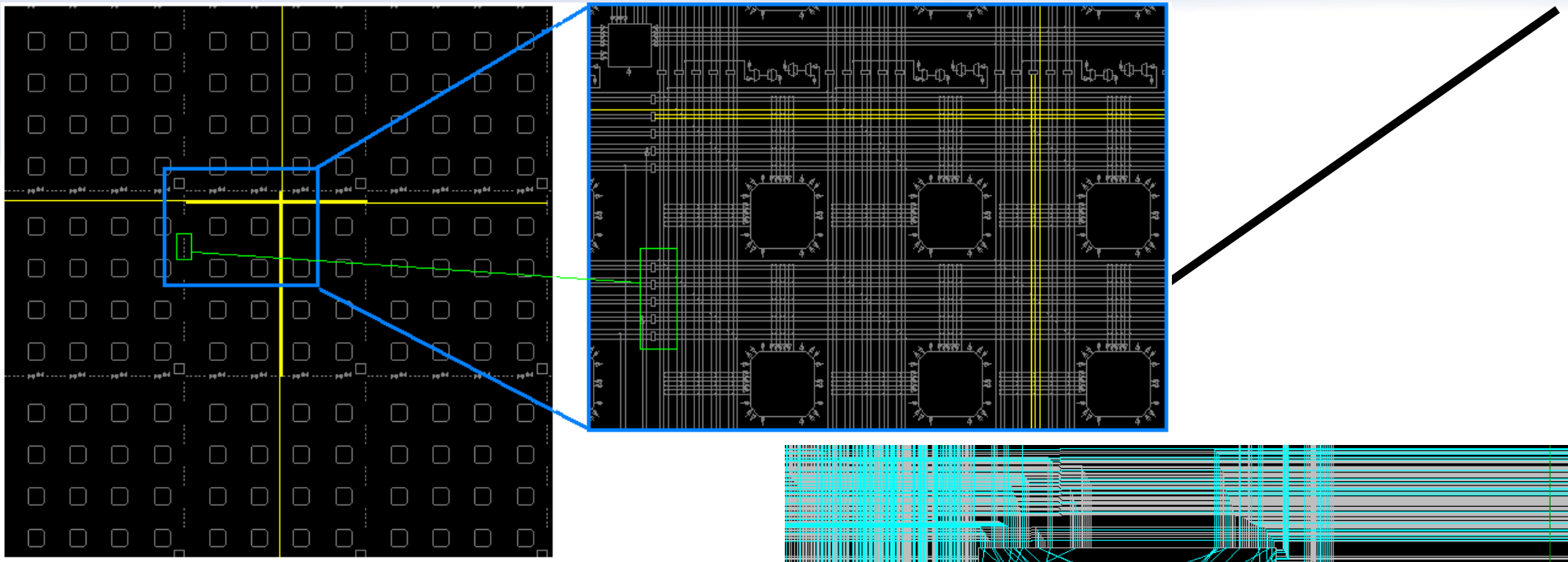
RocketIO GTX Transceiver, MAC Ethernet, PCI Express, MAC DSP, 2 PPC440 (not hardened)

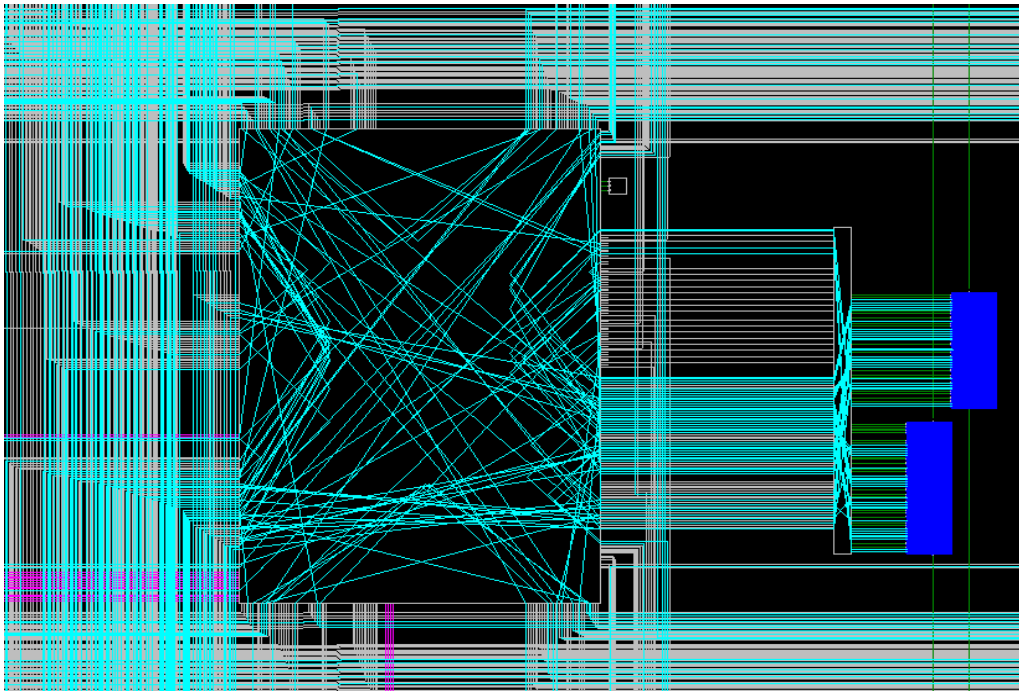
Logic capacity of the two FPGAs :

Virtex-5
ATF280E



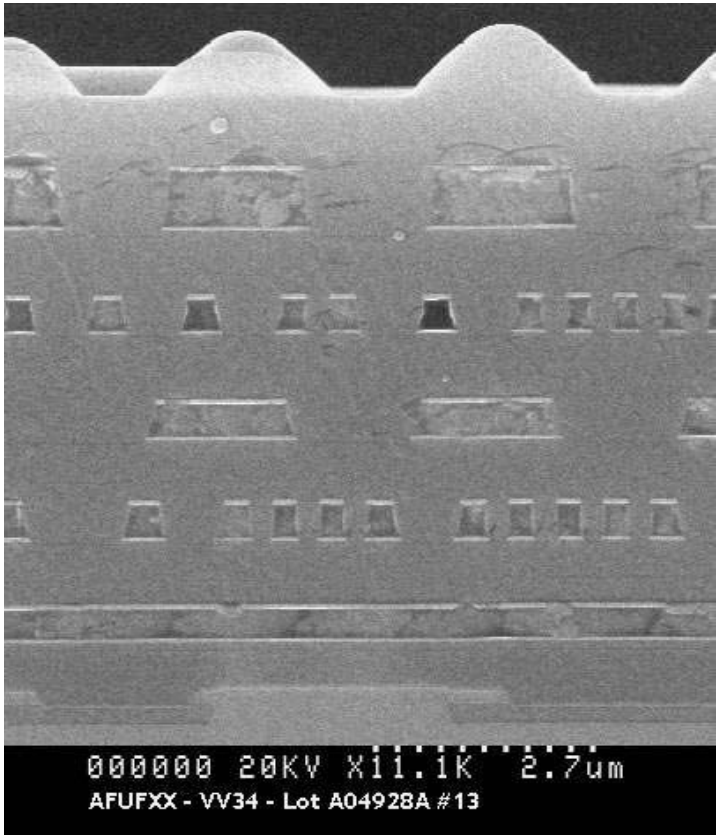
Routing resource of the two FPGAs





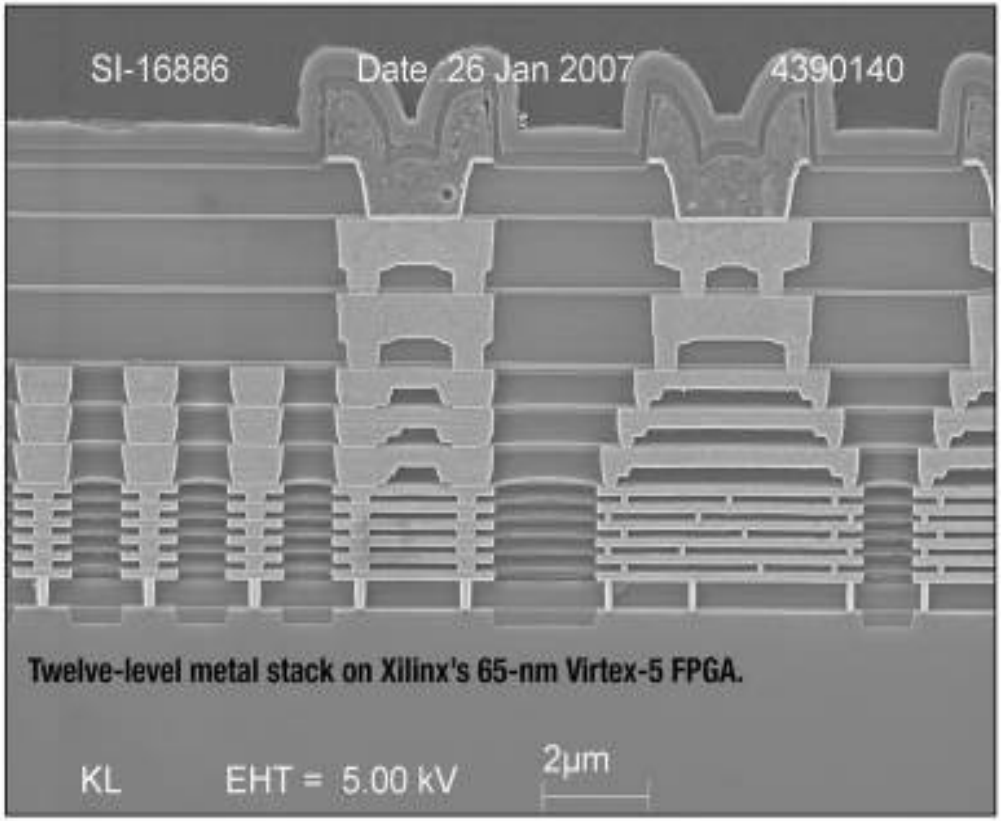
Process comparison

ATF280E : **0.18µm** CMOS technology



AT58KRHA (180 nm - 6 metal layers)
same as ATC18RHA ASIC

Virtex-5 : **65-nm** (triple oxide process)



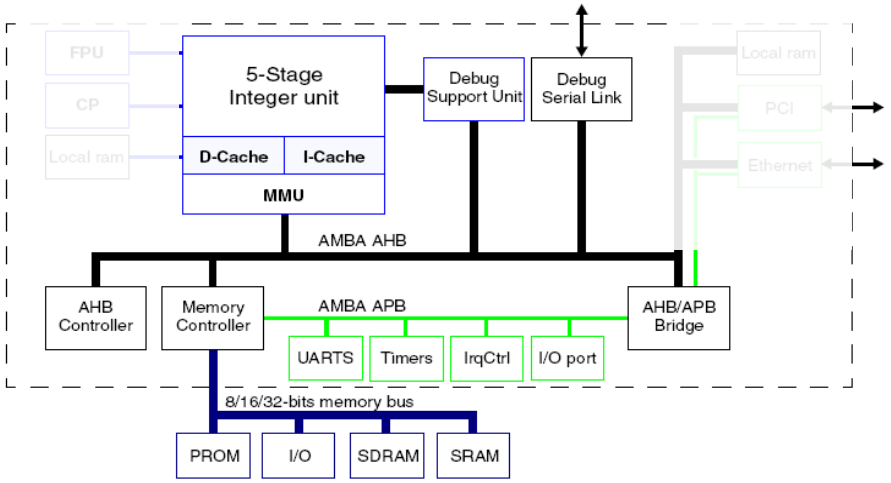
Virtex-5 (65 nm -12 metal layers)

ATMEL ‘s development tools

→ **Many difficulties encountered with the Atmel’s tools**

→ **The comparative evaluation of the two FPGAs has turned into an evaluation of the Atmel’s tools**

ATMEL ‘s development tools



Synthesis :

Comb cells : 110%

Seq Cell : 15 %

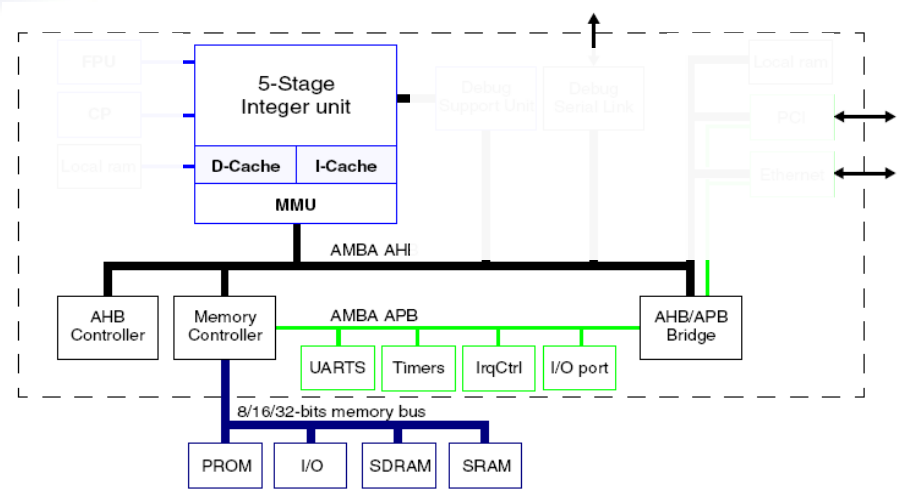
→ Leon2 ≈ less than 40 K gates in an Asic

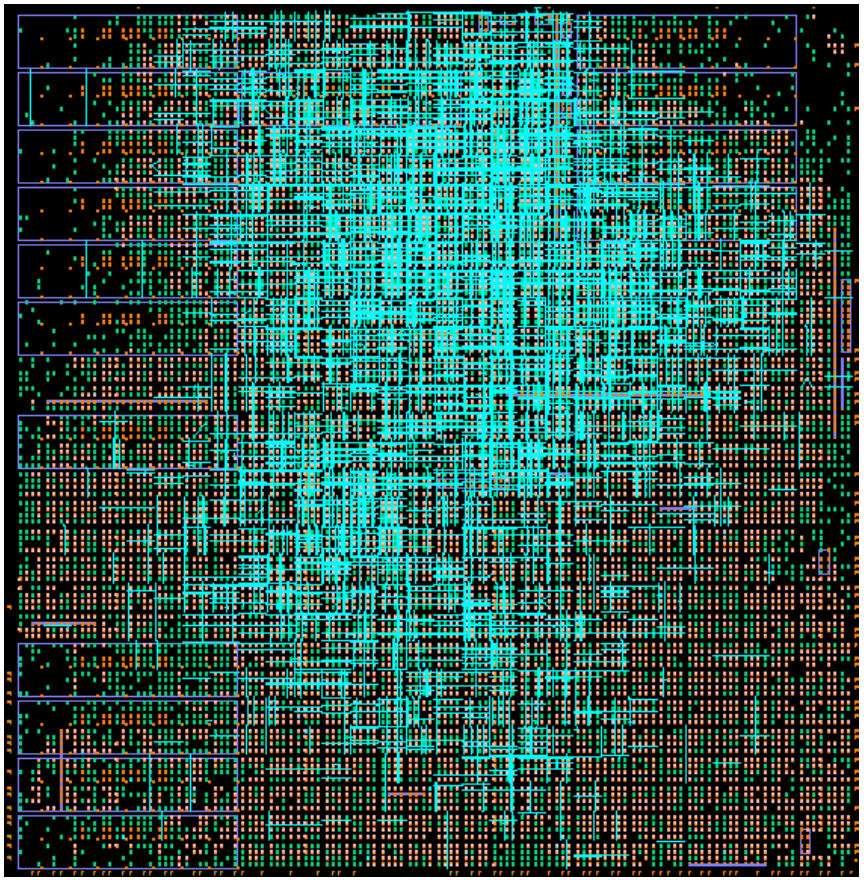
→ The same design in the SIRF (commercial version Virtex-5 FX130T) consumes 6 % LUT and 3 % Flip-Flop

Why does Leon not fit into the ATF280E ?

ATMEL ‘s development tools

And what about “Leon with no DSU” ?





Synthesis :

Comb cells : 82 %

Seq Cell : 12 %

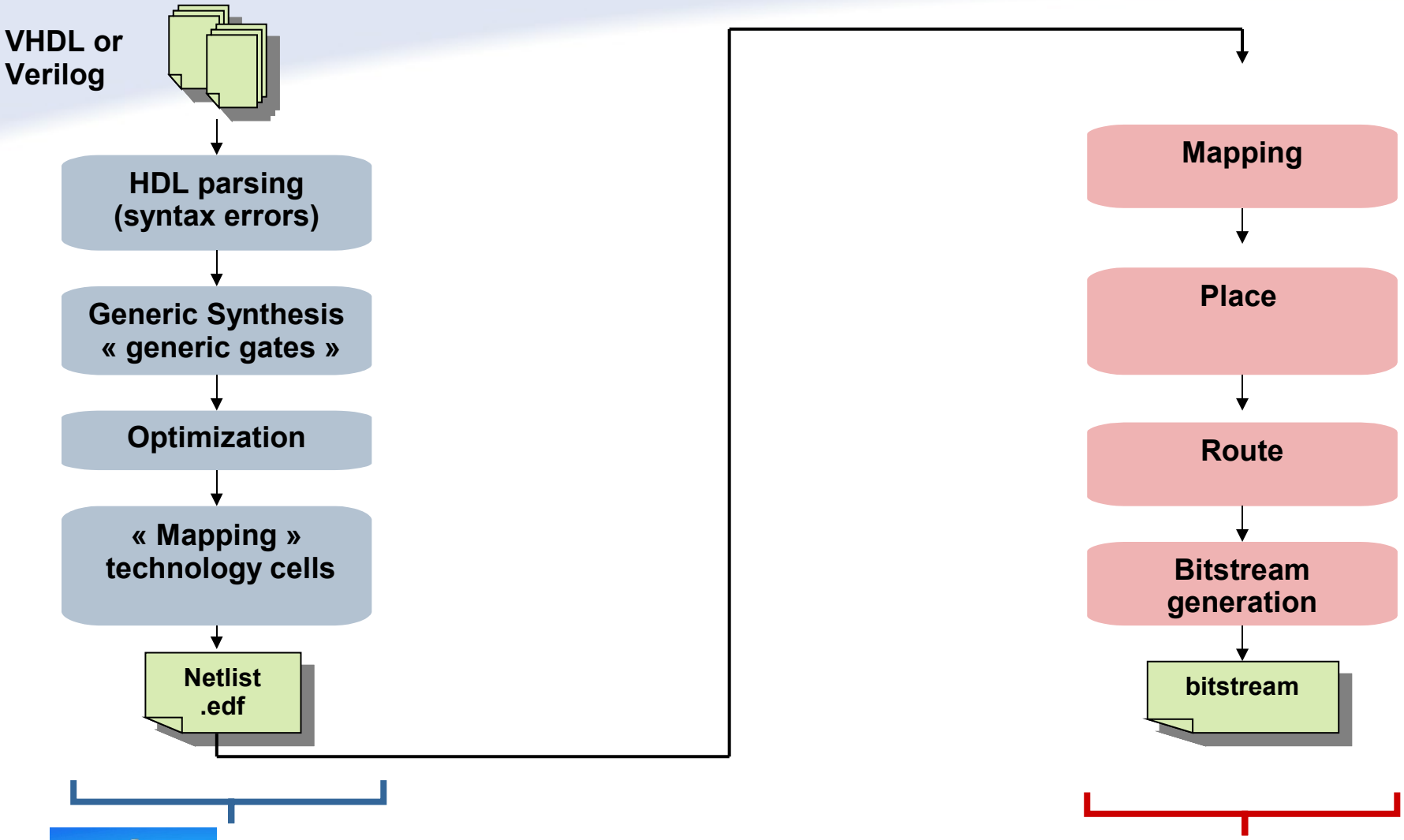
Place & Route : failed

Number of Cell Contentions : 588

Number of Net Contentions : 3675

It does not fit …

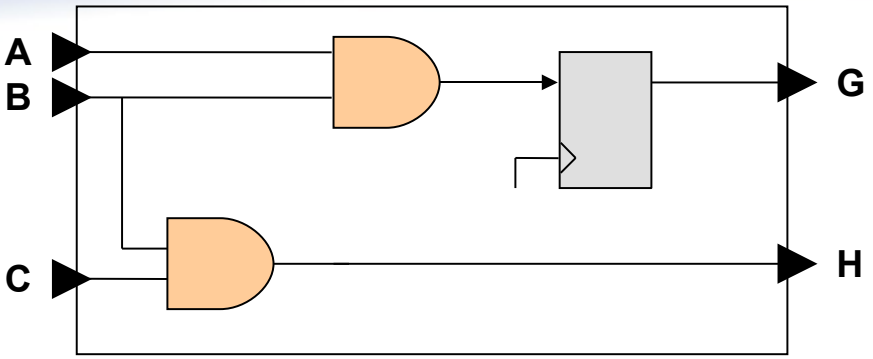
ATMEL ‘s development flow



The Macro detection problem : example

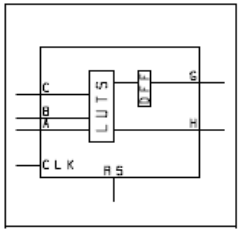
For example,

from this simple function



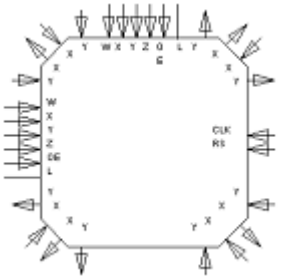
… the tool should

recognize



Macro « FGEN2R »

=

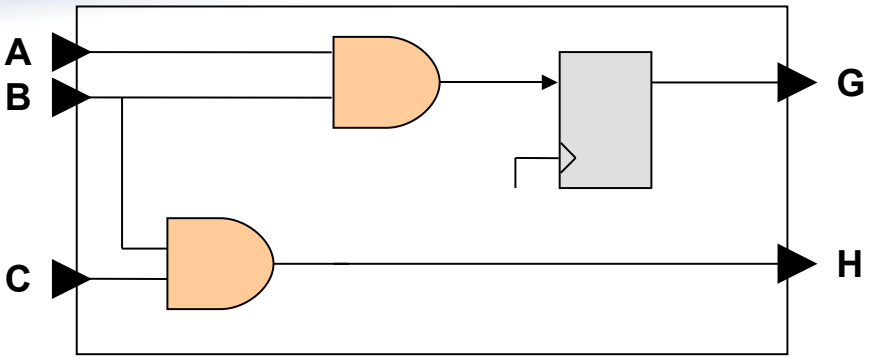


one Core Cell

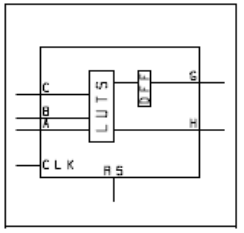
The Macro detection problem : example

For example,

from this simple function

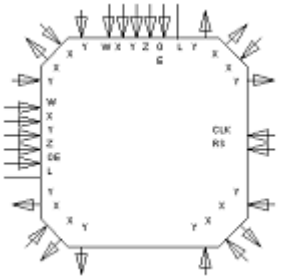


… the tool should recognize



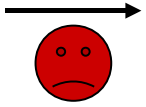
Macro « FGEN2R »

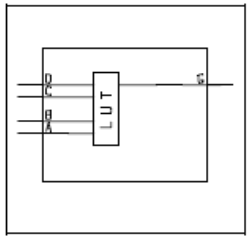
=



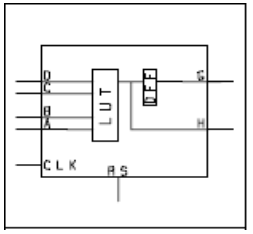
one Core Cell

… but instead, recognizes



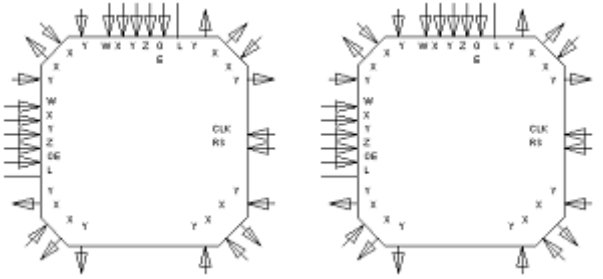


Macro « FGEN1 »



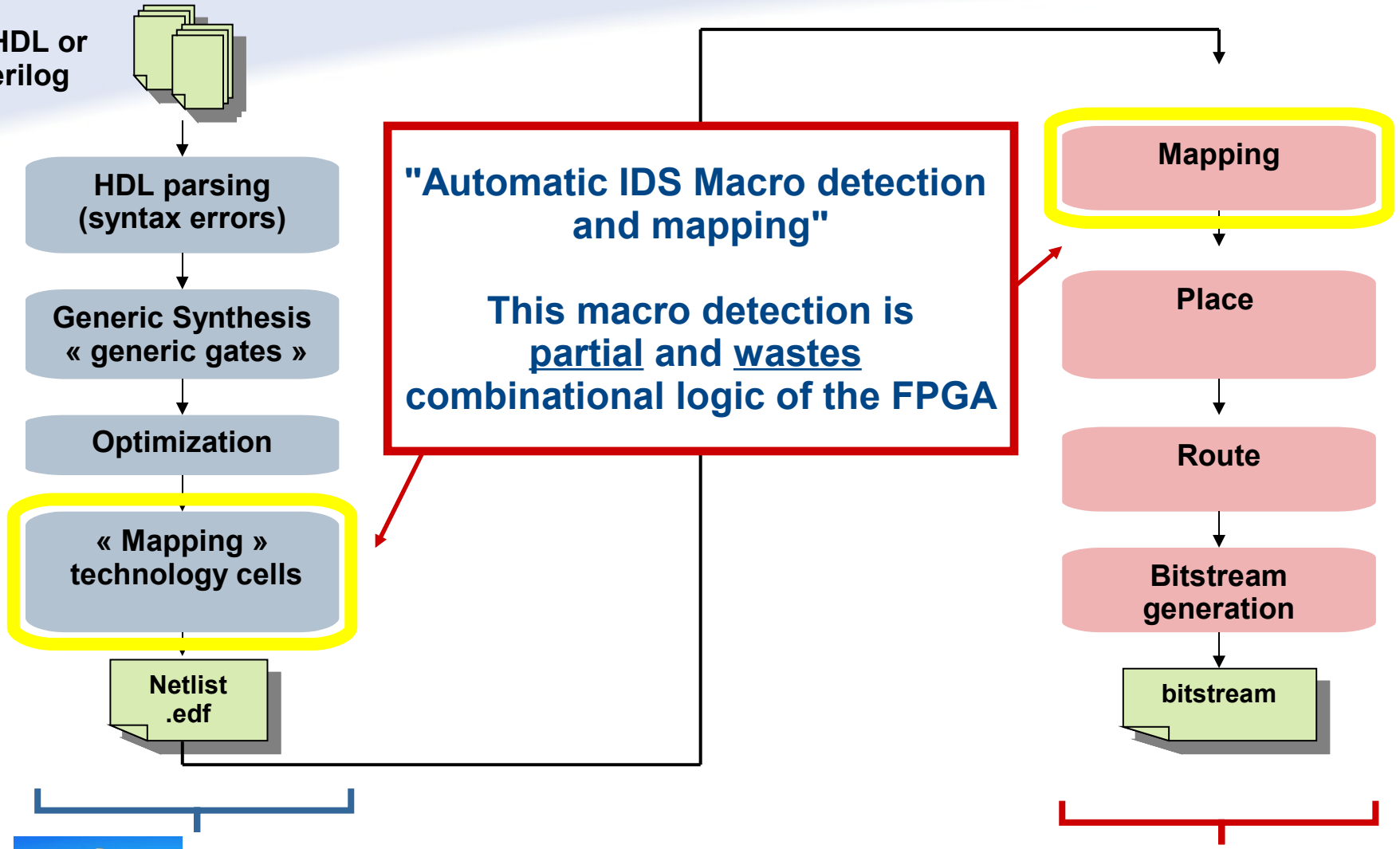
Macro « FGEN1R »

=

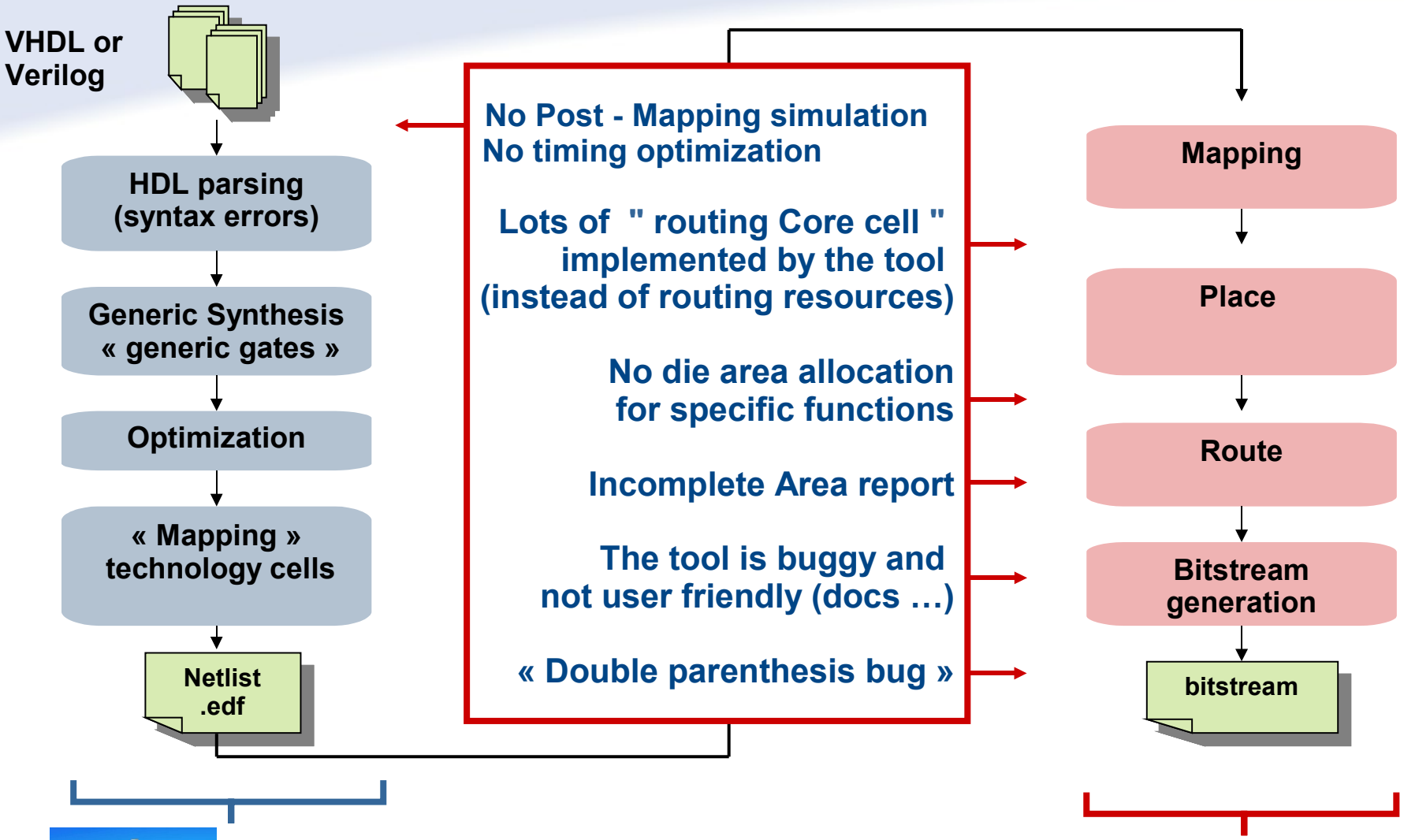


two Core Cells
+ routing resources

Atmel development flow : main issue



Atmel development flow : other issues

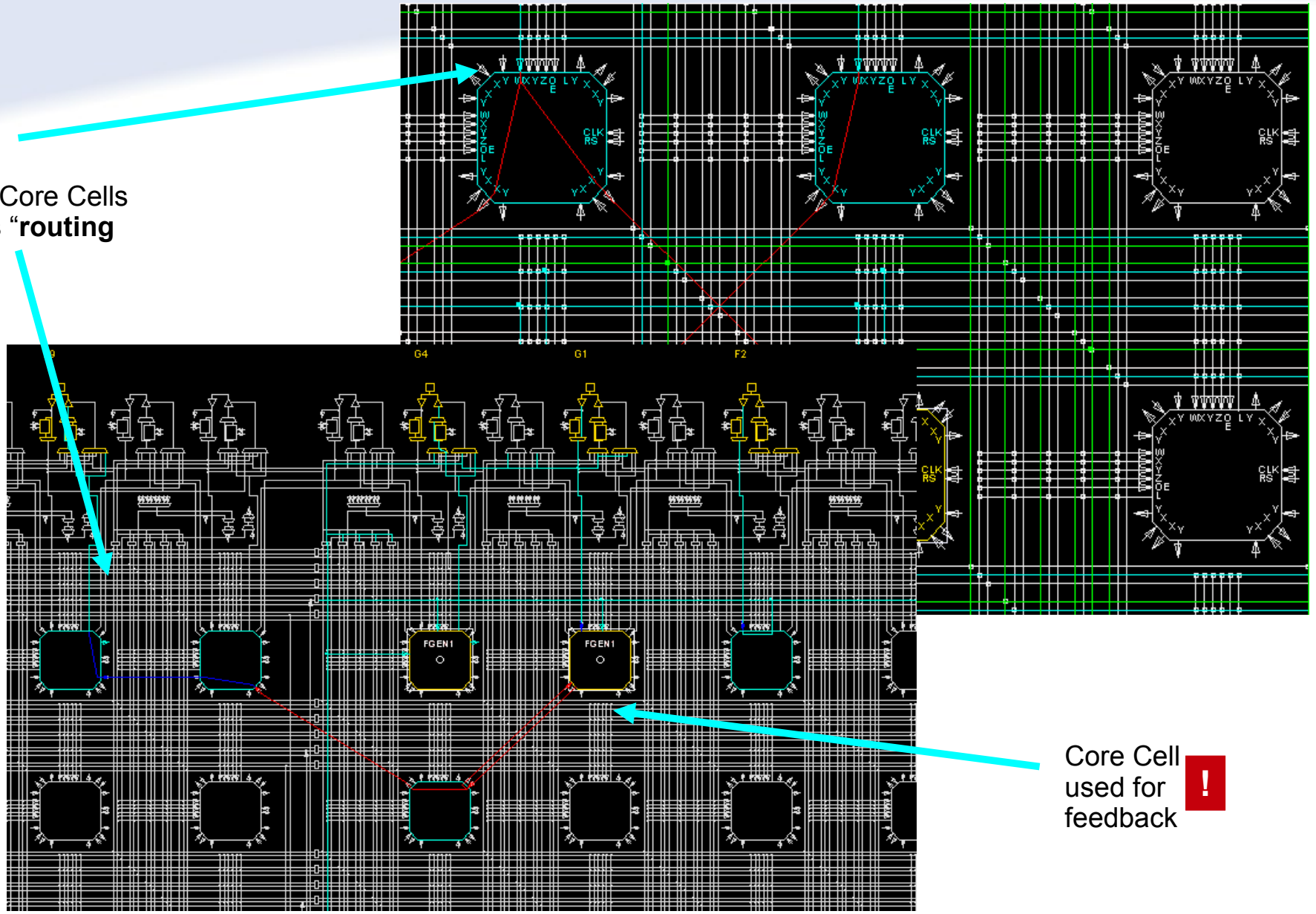


MENTOR Precision Synthesis

ATMEL Figaro IDS

Core Cell Waste : example

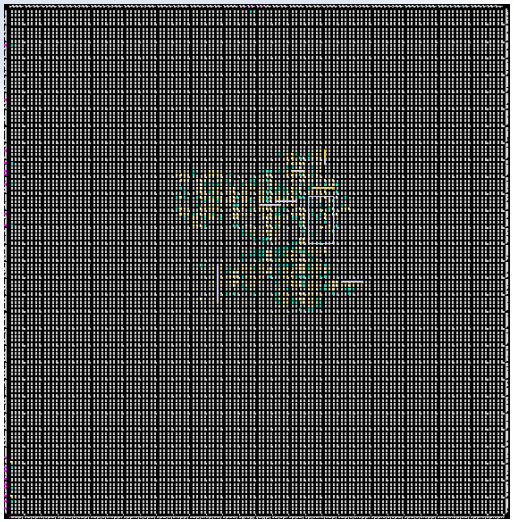
A lot of Core Cells used as “**routing Cell** “



Core Cell used for feedback

Part B : designs implemented

- **Space Wire UK VHDL IP** (with the LVDS drivers)

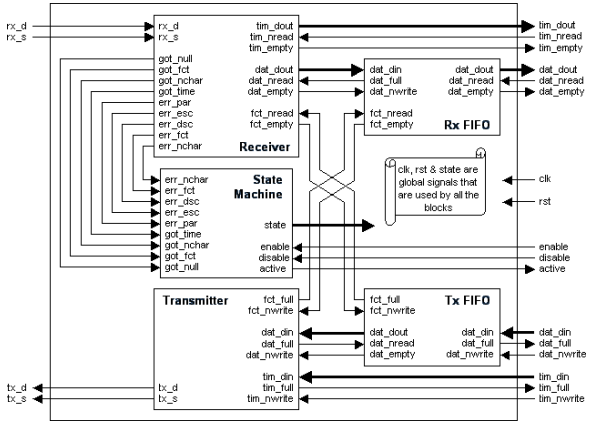


Synthesis :

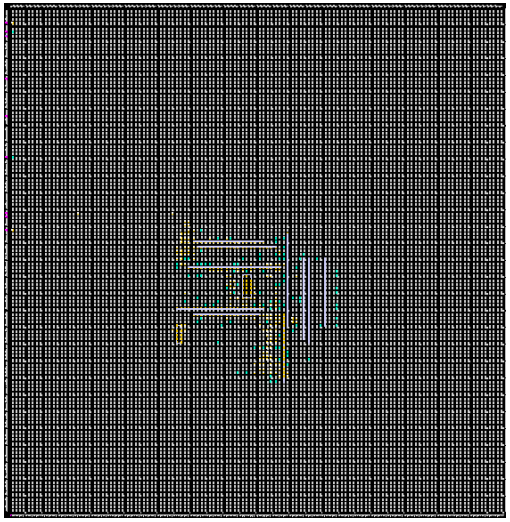
Combinational Cells : **4.3%**
Sequential Cells : **1 %**

P&R :

Logic Core Cells (512)
+ Routing Cells (138) : **4,5 %**



- **A recursive filter** + 2 serial/parallel converters



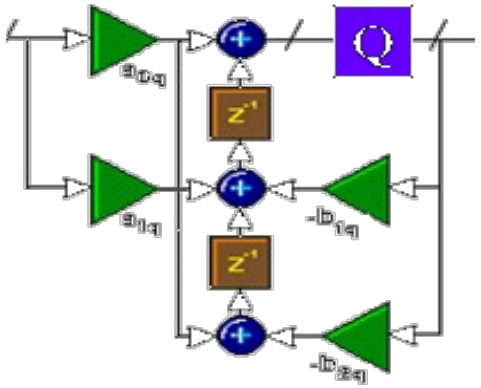
Synthesis :

Combinational Cells : **1,76%**
Sequential Cells : **0.86%**

P&R :

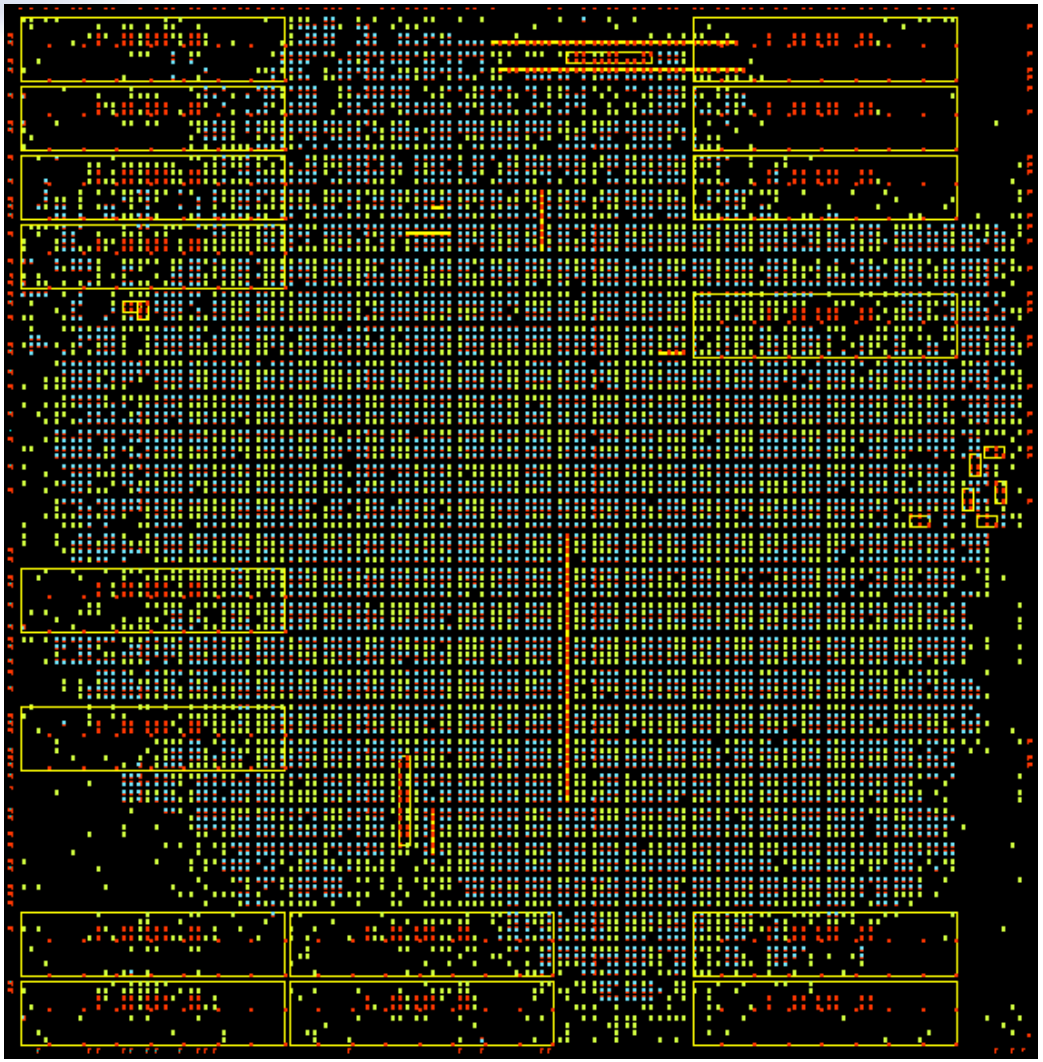
Logic Core Cells (377)
+ Routing Cells (92) : **3,3 %**

Max freq : Up to 50 MHz



Part B : designs implemented

- **Leon_mcore** (No DSU / code in bprom.vhd / IO access only)



Synthesis :

Combinational Cells	**56.3%**
Sequential Cells	**8 %**

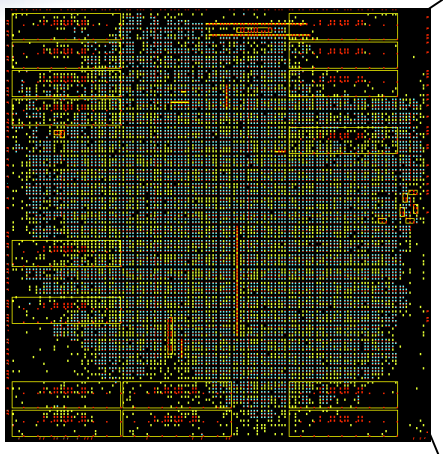
P&R :

Logic Core Cells + routing cells	**73,7 %**

→ **Max freq : 14,6 MHz**

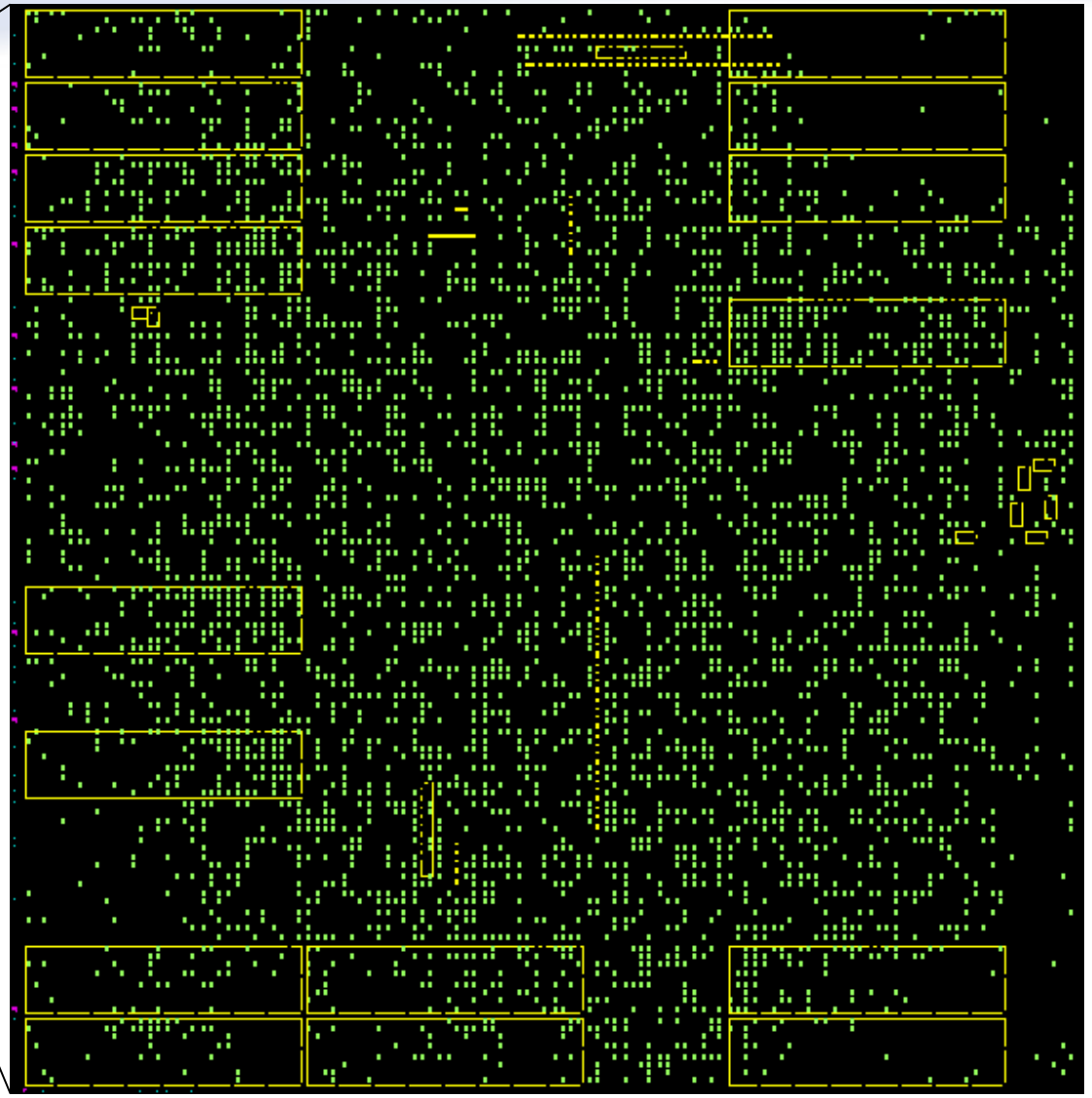
→ **3 hours of Place and Route**

Illustration of the routing cell issue



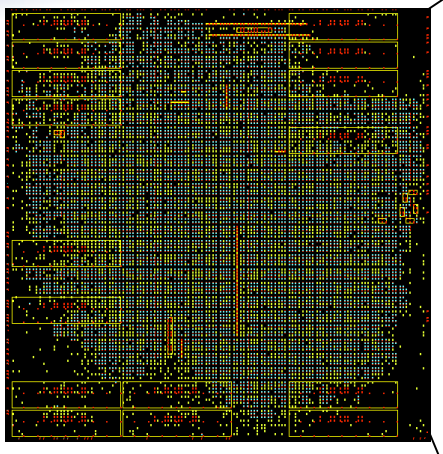
“Leon_mcore”

(Place & route OK, the design works)



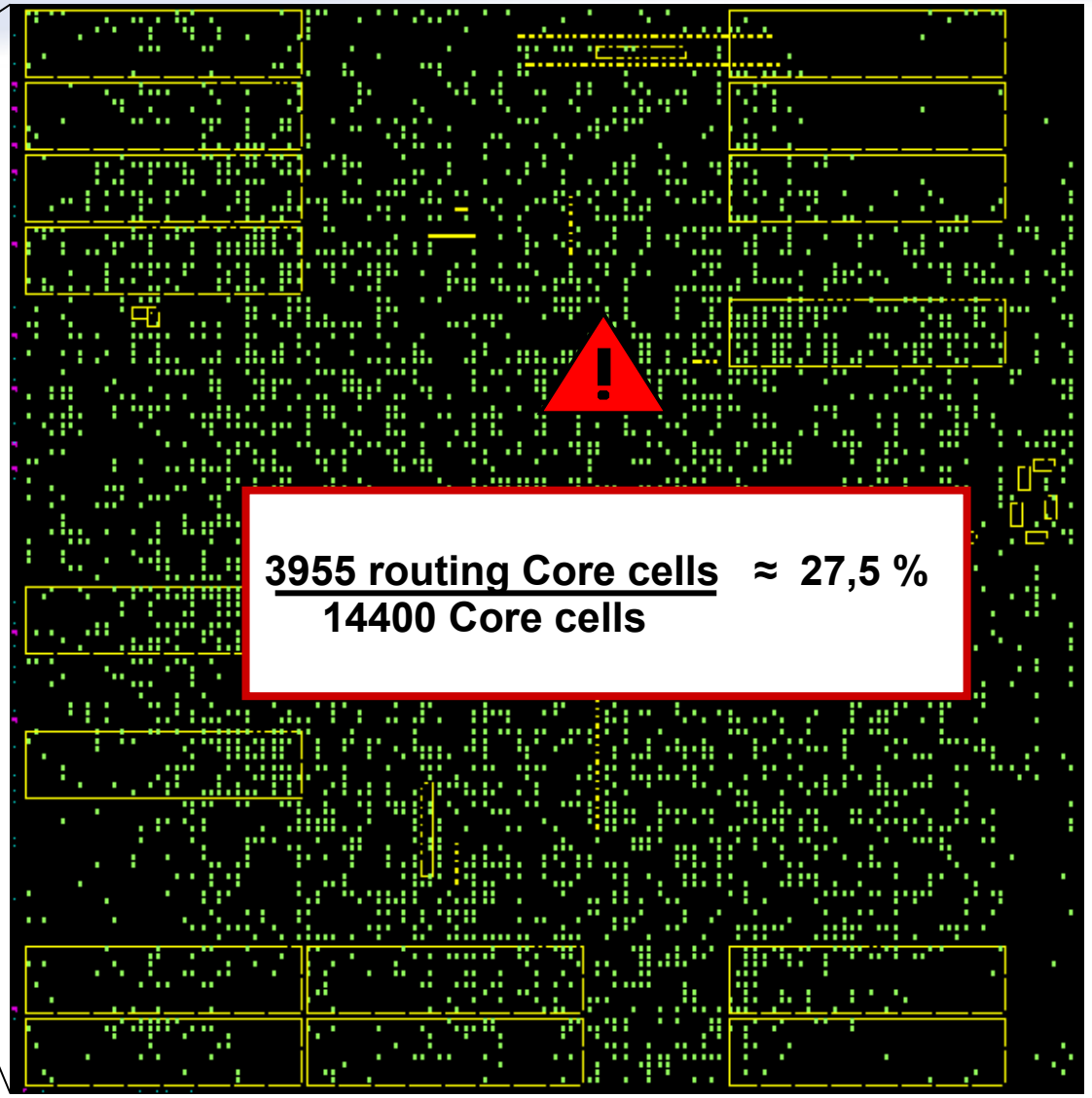
Green spots = Core Cells used as “routing cells”

Illustration of the routing cell issue



“Leon_mcore”

(Place & route OK, the design works)



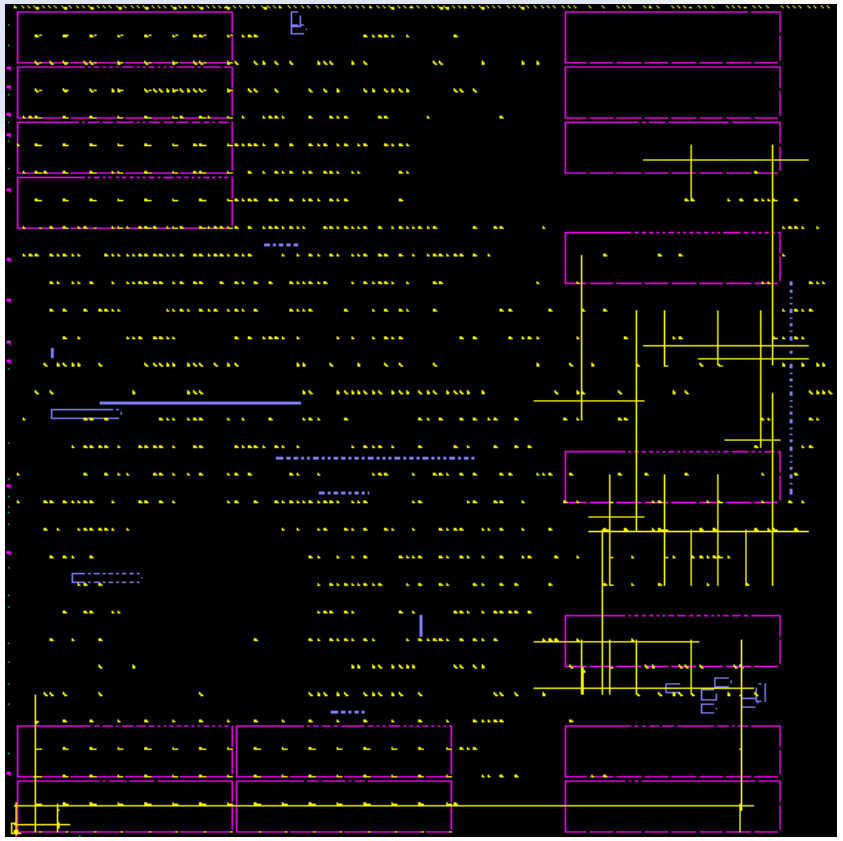
Green spots = Core Cells used as “routing cells”

An illustration of the issue reported by KDA : (Clk & Clkn of the mcore design)

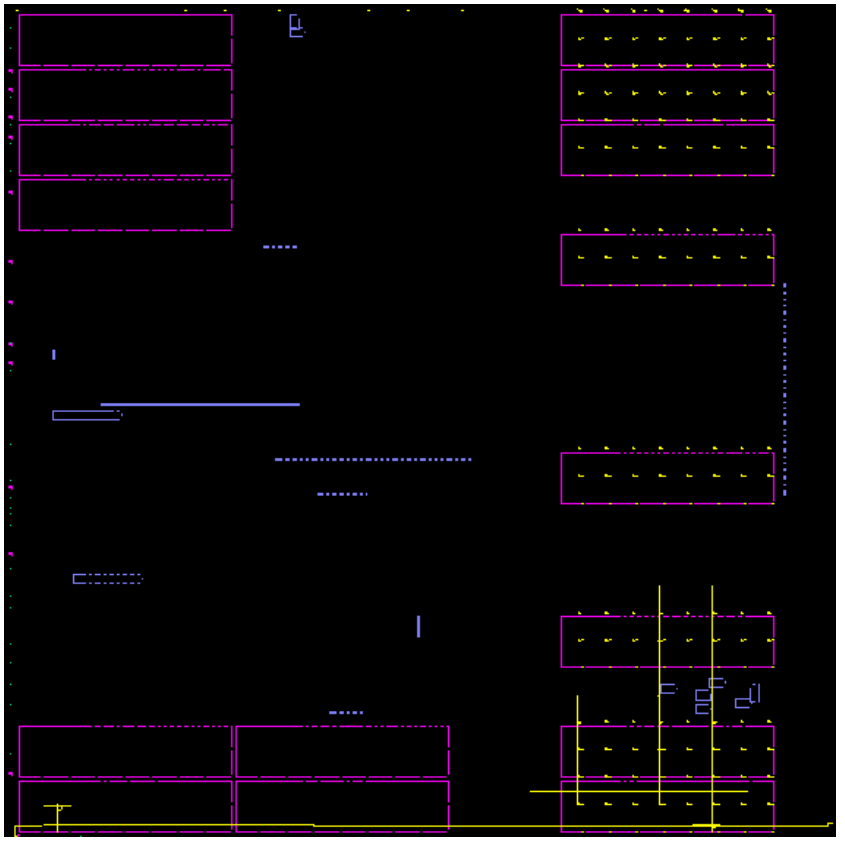
→ **Large clocks skew in the clock trees in the case of a design containing derived clocks**

→ **Figaro does not report correctly the timing problems**

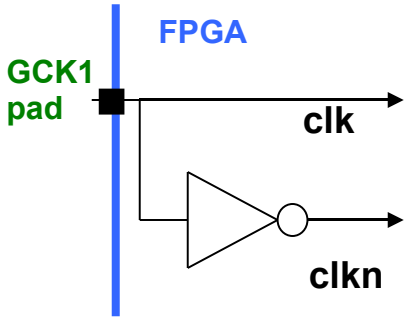
An illustration of the issue reported by KDA : (Clk & Clkn of the mcore design)



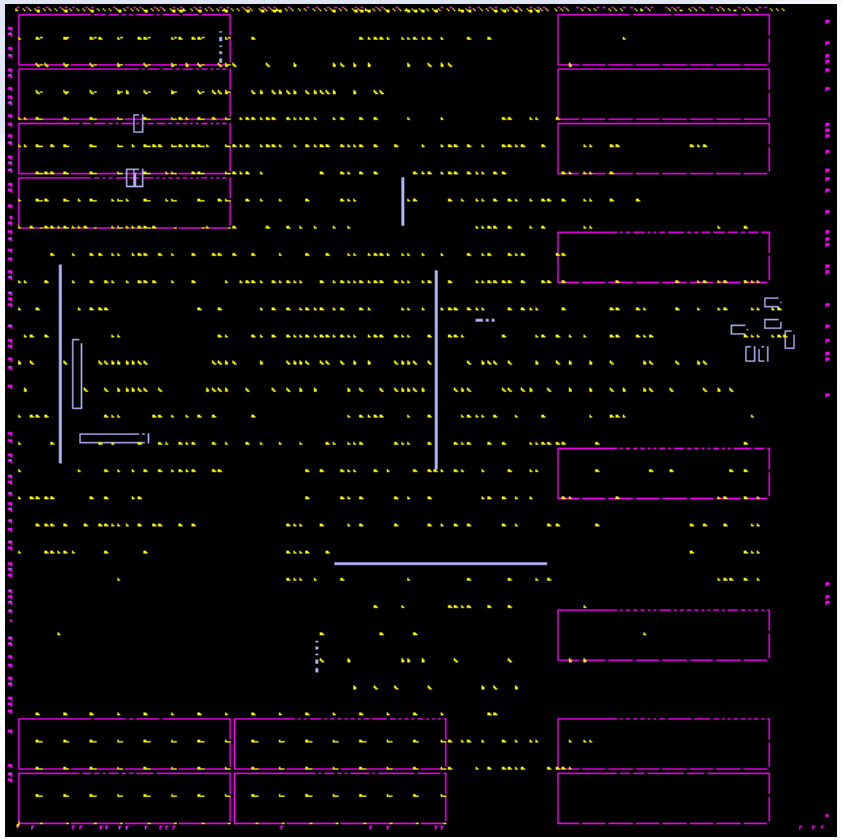
The net “clk” (the main external clock)



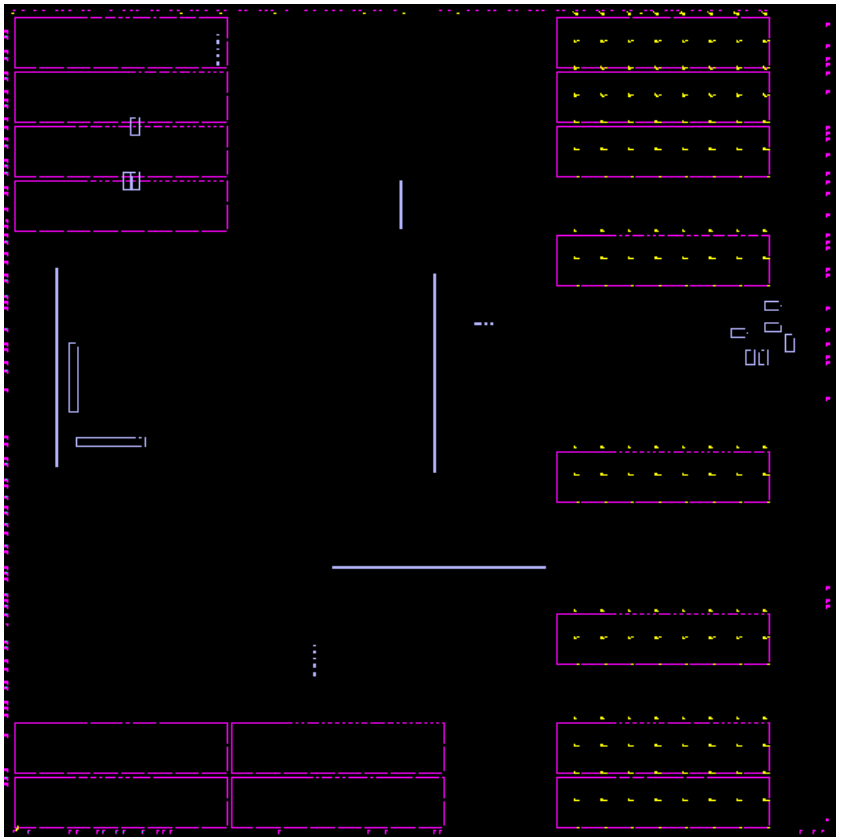
The net “clkn” (the derived clock)



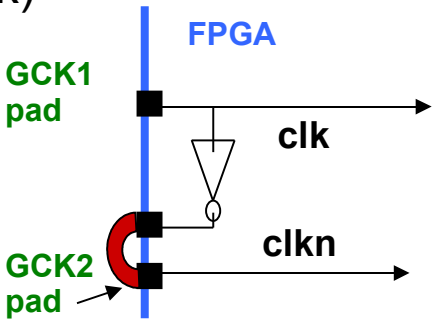
An illustration of the workaround found by KDA :



The net “clk” (the main external clock)



The net “clkn” (external now)



Conclusion :

→ Technology gap between Atmel and Xilinx (eg : routing resources)

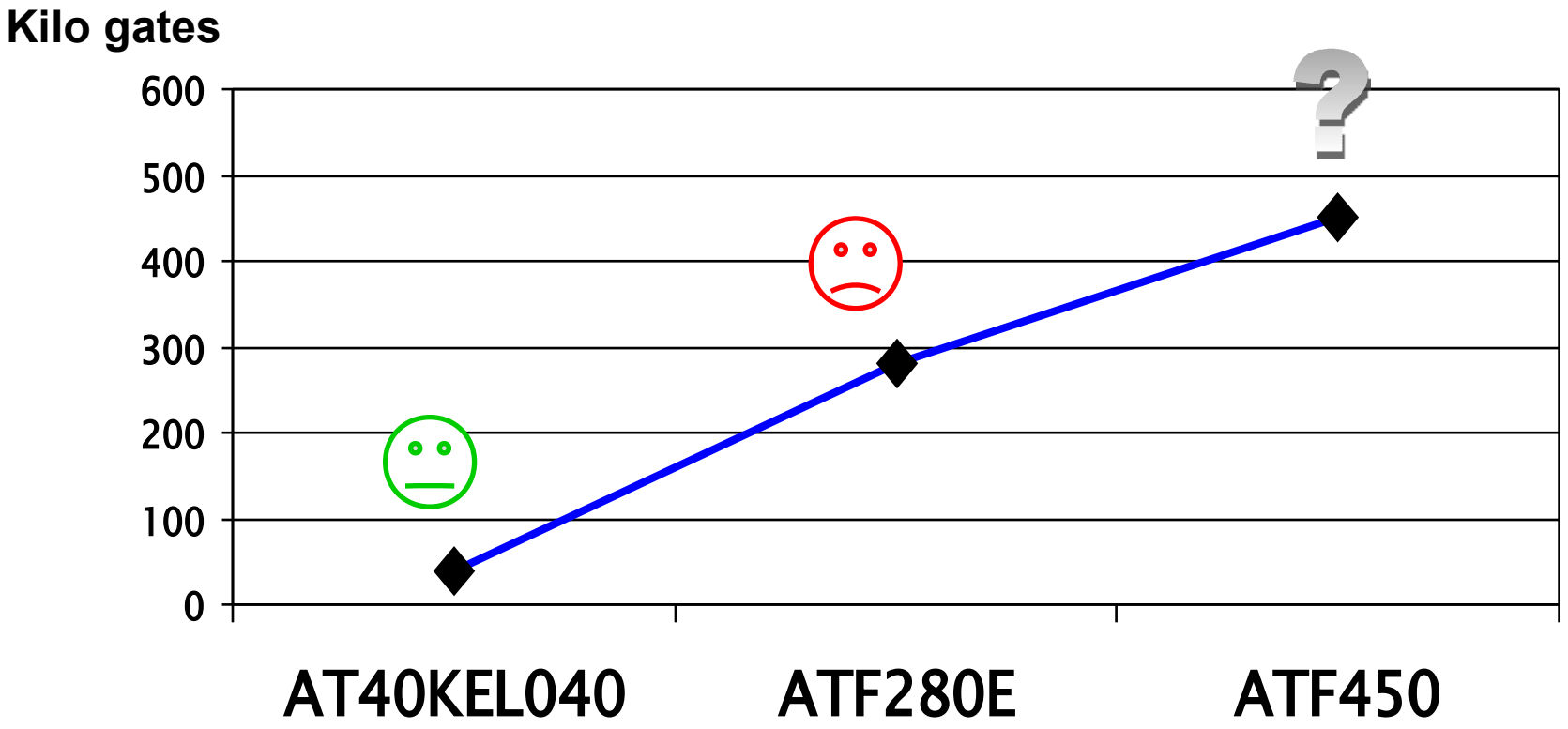
→ Nevertheless, Atmel FPGAs have a real potential (not ITAR, availability)

→ Poor documentation and immaturity of the tool

→ Space FPGA Designer appears to be the root cause of limitation and waste!

Conclusion :

Will the tool support up the next Atmel ‘s FPGAs ?



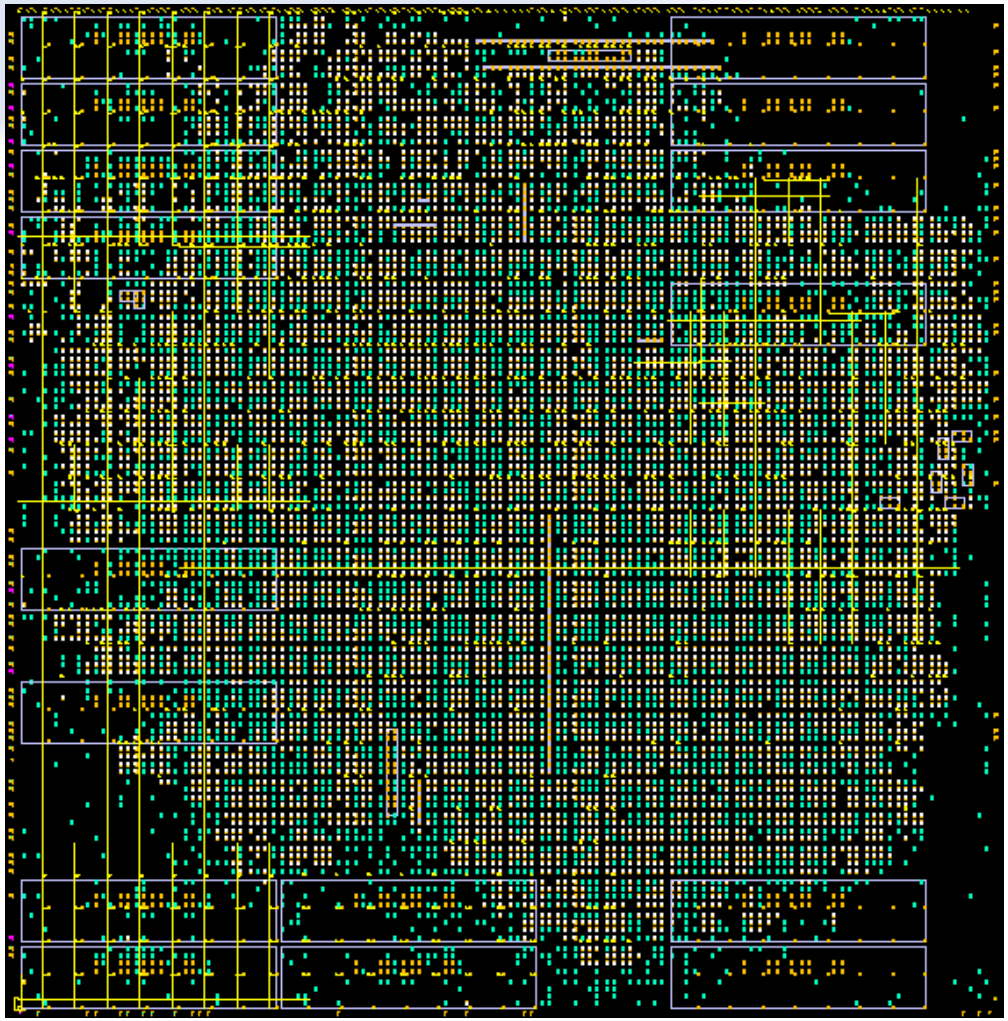
Thanks very much,

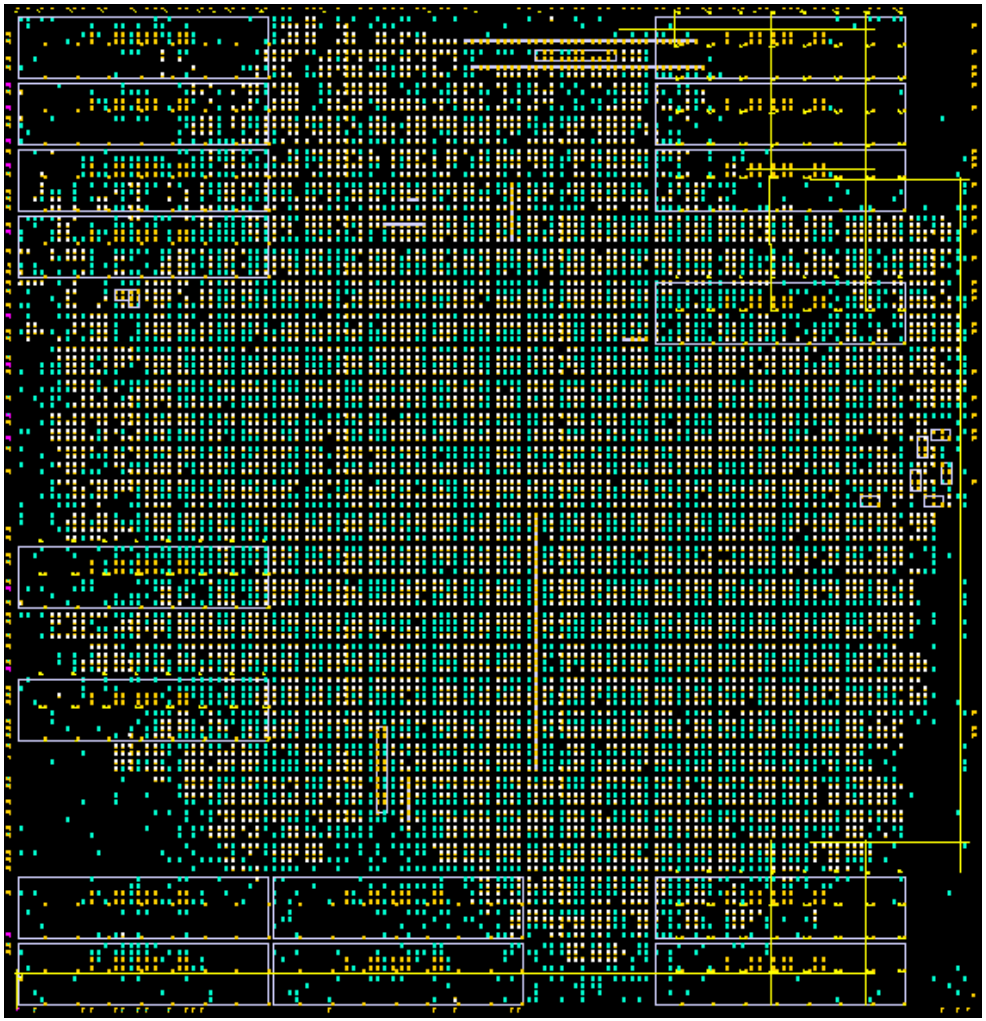
Do you have any questions ?

Add-On Slides

An illustration of the issue reported by KDA : (Clk & Clkn of the mcore design)

Add-on Slides





The net “clk” (the main external clock)

The net “clkn” (the derived clock)

Primitives inferred for combinational Logic : the “second mapping” step

Add-on Slides

for the main combinational glue of a design :

✖→ no recognition of those macros

Table 6 describes the dynamic macros available in the PSLI library.

Table 6. Logical Function

Logical Function	Description
FGEN1	*n* input function generator (1 ≤ *n* ≤ 4)
FGEN1F	*n* input function generator with combinatorial feedback (1 ≤ *n* ≤ 3)
FGEN1FT	*n* input function generator with combinatorial feedback followed by tri-state buffer (1 ≤ *n* ≤ 3)
FGEN1R	*n* input function generator followed by a register (1 ≤ *n* ≤ 4)
FGEN1RF	*n* input function generator with registered feedback (1 ≤ *n* ≤ 3)
FGEN1RFT	*n* input function generator with registered feedback followed by tri-state buffer(1 ≤ *n* ≤ 3)
FGEN1RT	*n* input function generator followed by a register and tri-state buffer (1 ≤ *n* ≤ 4)
FGEN1T	*n* input function generator followed by a tri-state buffer (1 ≤ *n* ≤ 4)
FGEN2	Two *n* input function generators (1 ≤ *n* ≤ 3)
FGEN2F	Two *n* input function generators with combinatorial feedback on 1-output(1 ≤ *n* ≤ 2)
FGEN2FT	Two *n* input function generators with combinatorial feedback followed by tri-state buffer on 1-output (1 ≤ *n* ≤ 2)
FGEN2R	Two *n* input function generators with 1-output registered and the other combinatorial (1 ≤ *n* ≤ 3)
FGEN2RF	Two *n* input function generators with 1-output registered and feedback (1 ≤ *n* ≤ 2)
FGEN2RFT	Two *n* input function generators with 1-output registered, tri-stated and feedback (1 ≤ *n* ≤ 2)
FGEN2RT	Two *n* input function generators with 1-output registered and tri-stated (1 ≤ *n* ≤ 3)
FGEN2T	Two *n* input function generator with 1-output tri-stated (1 ≤ *n* ≤ 3)
MGEN(1)	Two *3*-input function generators
MGENR	Two 3-input function generators with 1-output registered
MGENRT	Two 3-input function generators with 1-output registered and tri-stated
MGENT	Two 3-input function generator with 1-output tri-stated

Note: 1. The MGEN macros are special case macros (typically used in multipliers) with an upstream AND gate feeding the Look-Up Tables.

[See slide 12]

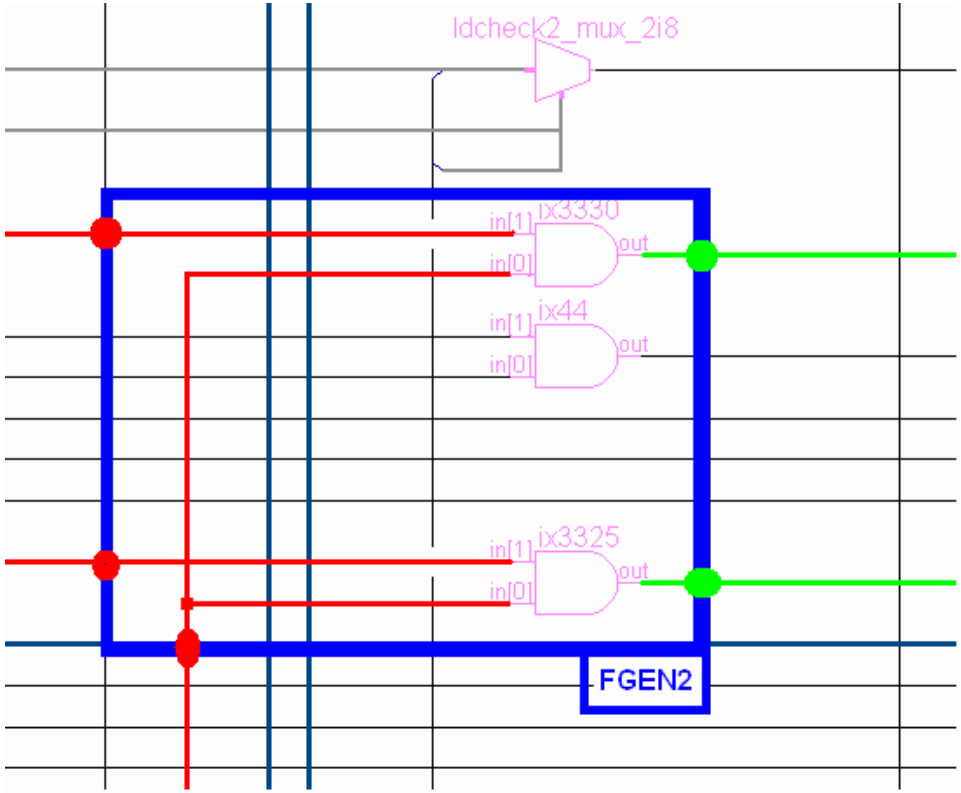
for the main combinational glue of a design :

→ Mapping of those macros only.

Cause of the partial macro detection : which mapping ?

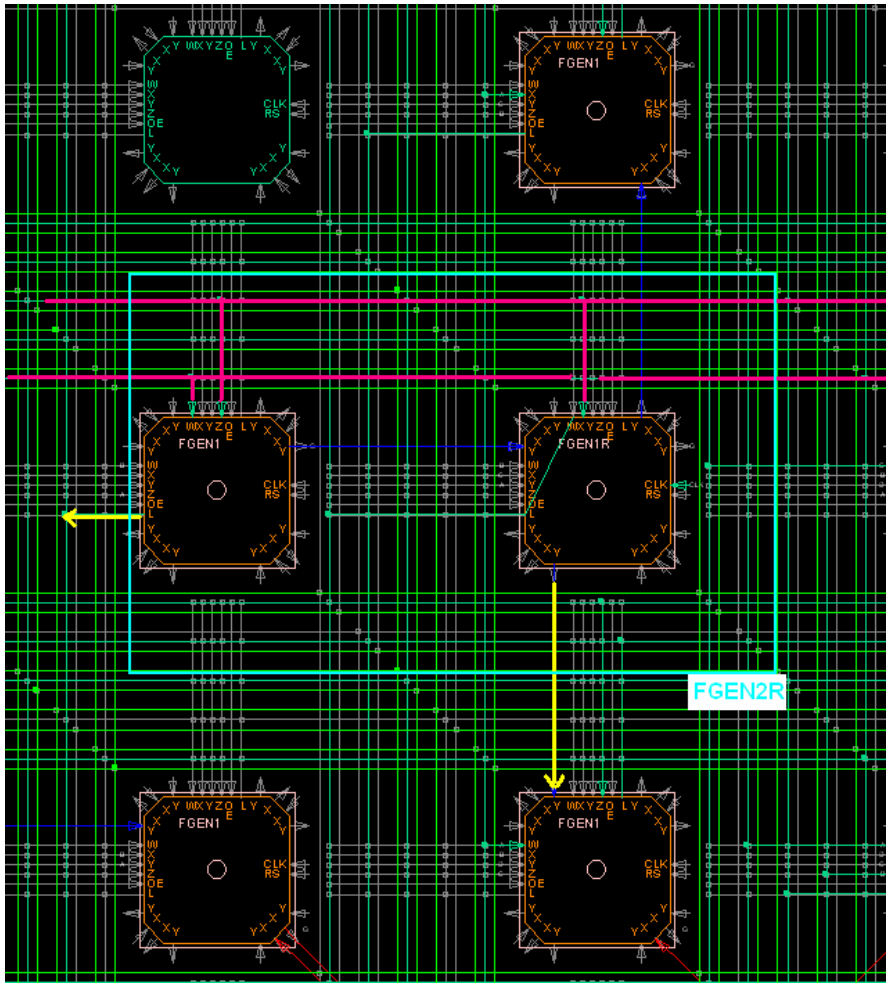
Potential recognition of a FGEN2

at the “synthesis mapping step” :



Potential recognition of a FGEN2R

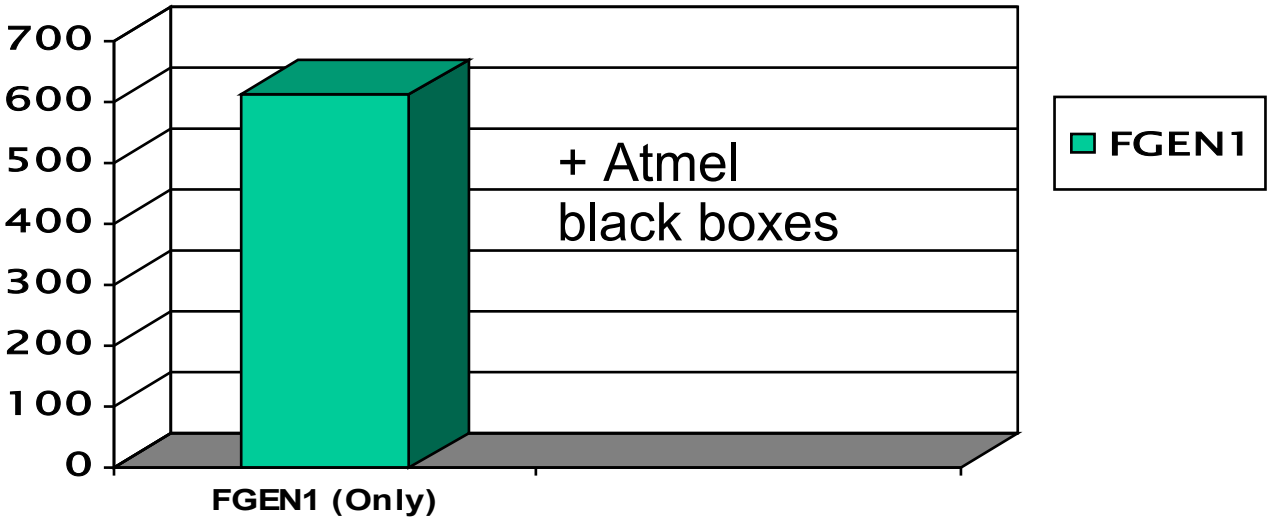
at the “Place and Route mapping step” :

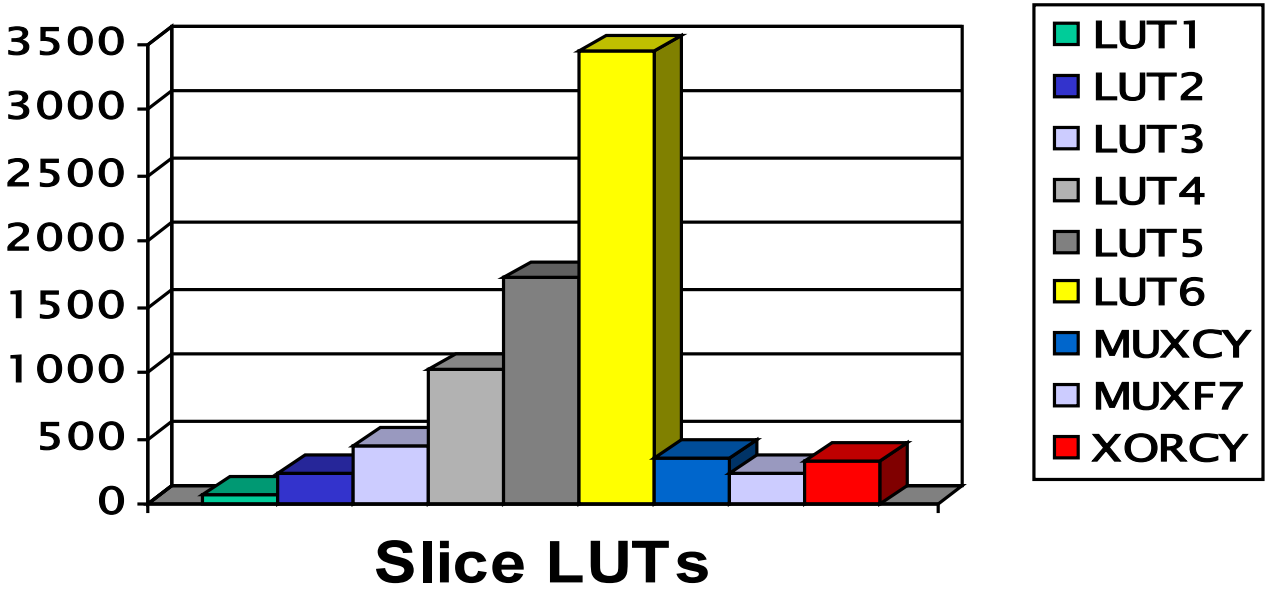


Primitives inferred for combinational Logic : synthesis step

Add-on Slides

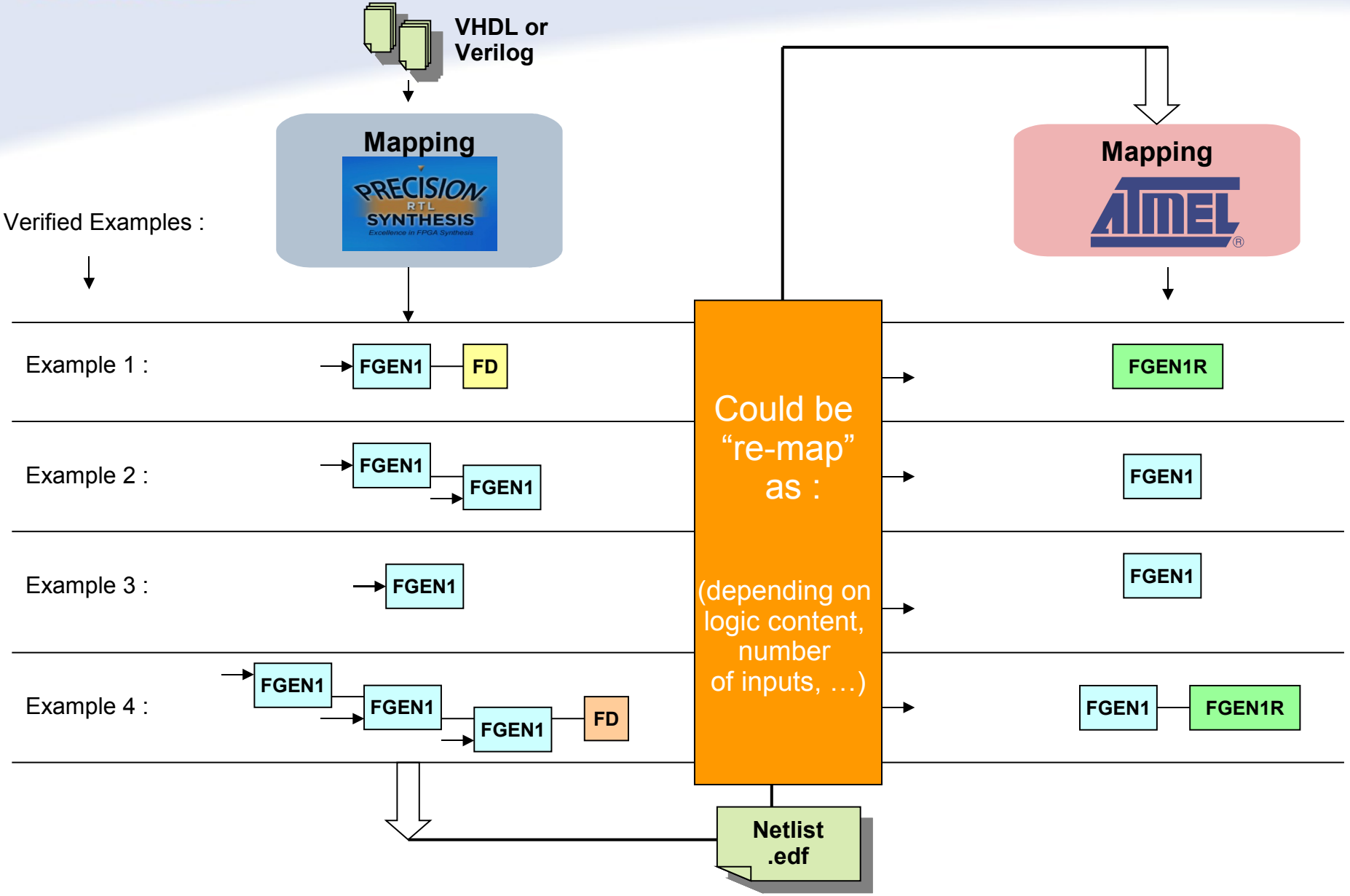
The Leon2 design :





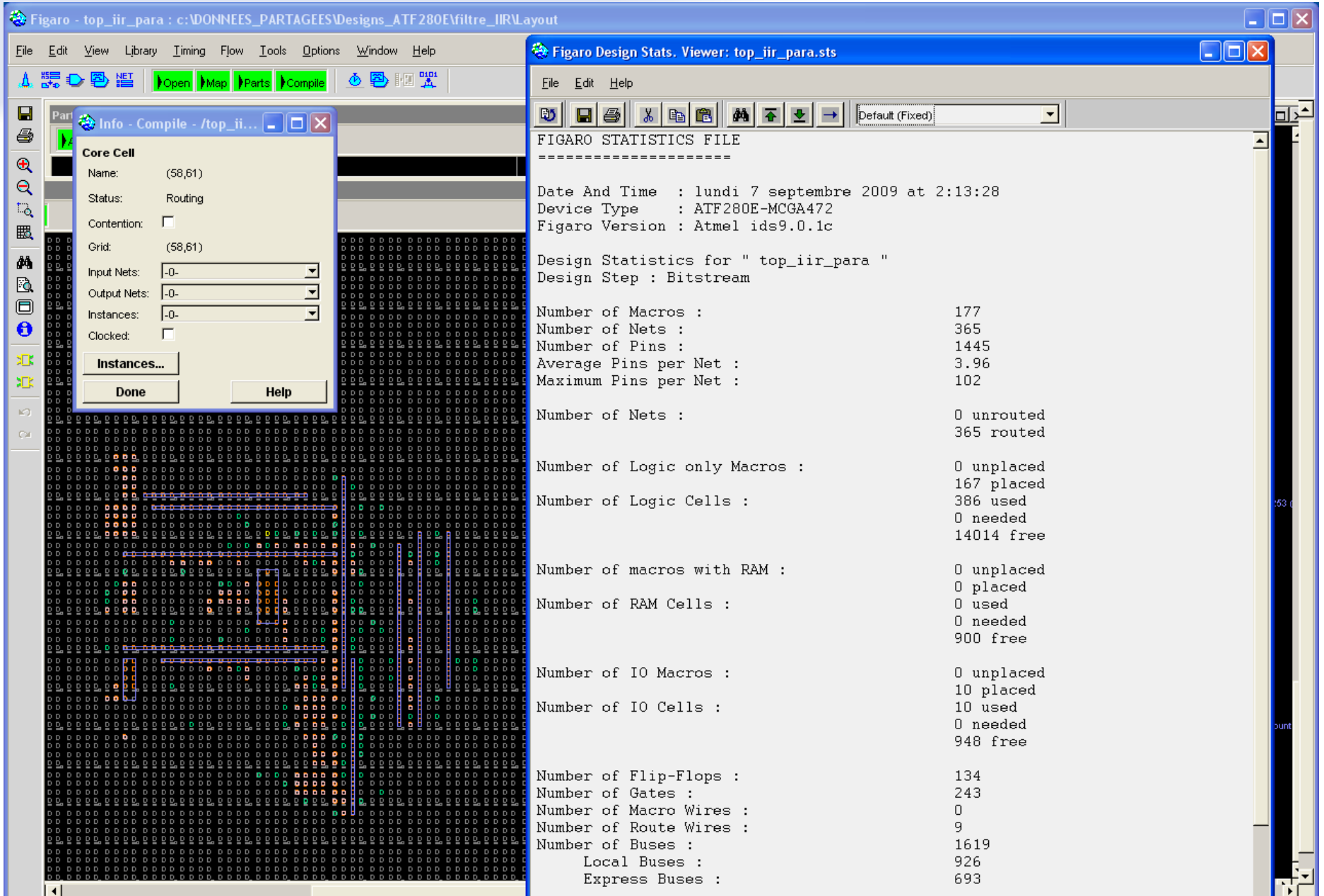
Mappings : between Mentor and Atmel

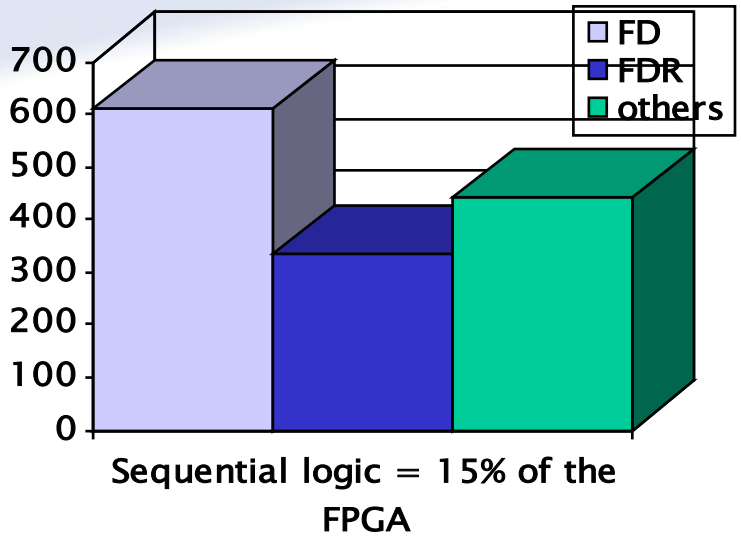
Add-on Slides



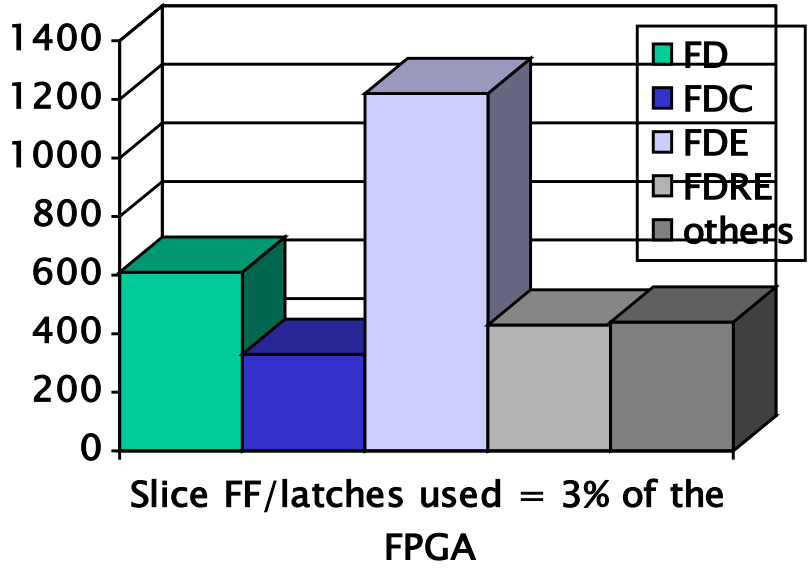
incomplete Area report

Add-on Slides





Sequential logic = 15% of the FPGA

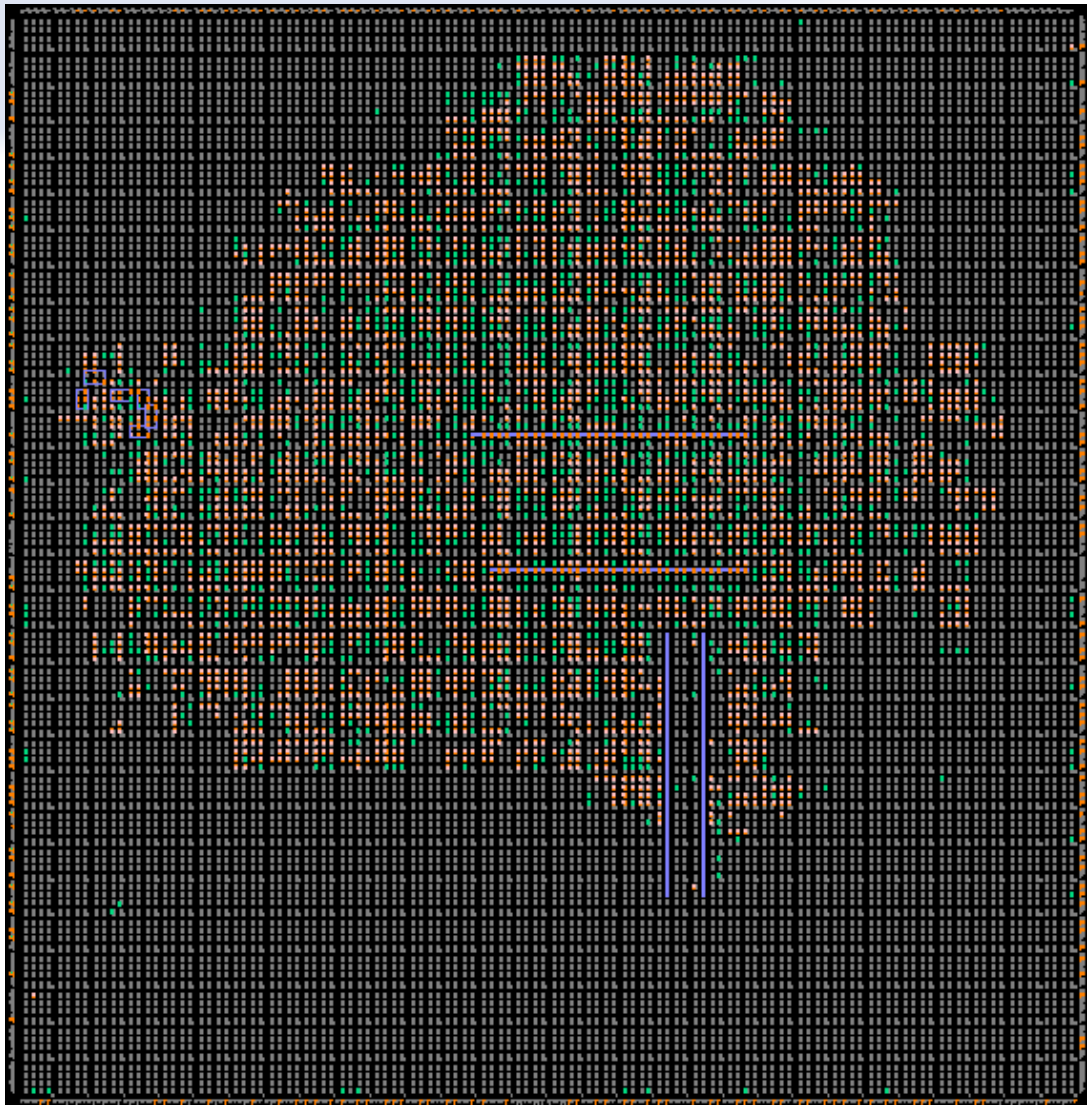


Slice FF/latches used = 3% of the FPGA

(There is no Clock Enable on the Atmel ‘s flip-flops)

Essais LEON2 : implantation d'1 l'IU

Add-on Slides



Synthesis :

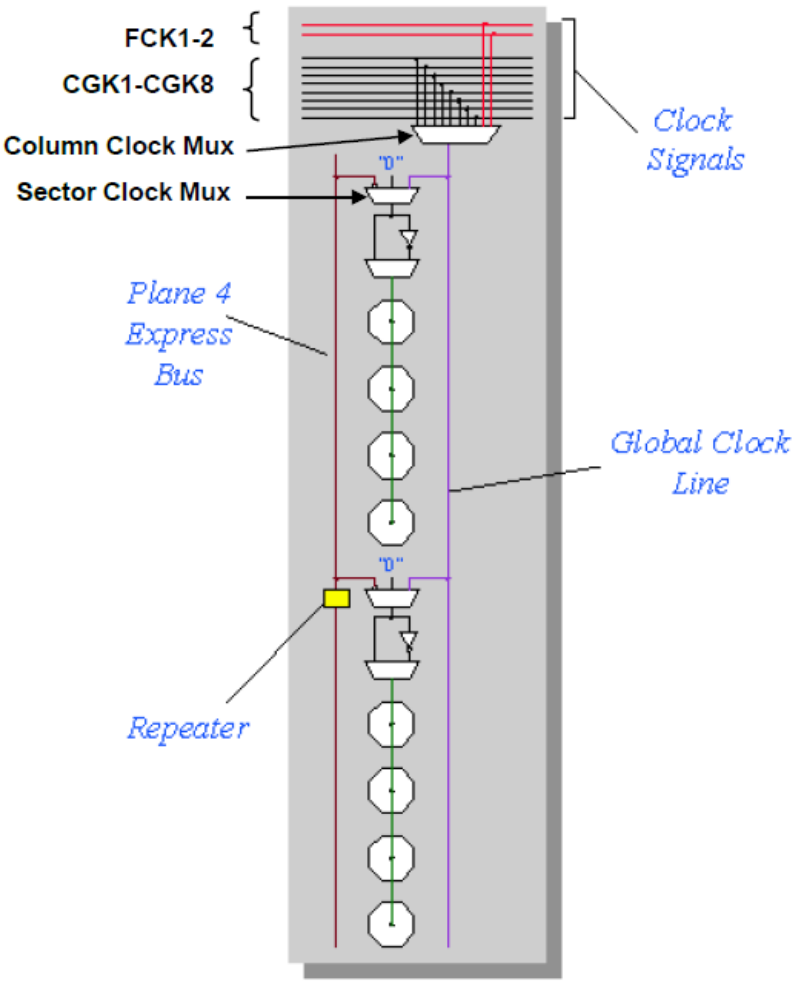
Combinational Cells : **30.06%**
Sequential Cells : **3.88%**

P&R :

Logic : Core Cells (3641)
+ 343 Route Wires used = **27,6 %**

Atmel clock distribution (src : ATMEL)

Global & Fast Clocking



8 Dedicated 'Global Clock buses'

- Individual 'Global Clock' line feeds all the logic cells in one column
- GCK1 to GCK8
- Distributed across a special high-speed bus (top edge of the FPGA)
  - => FPGA distribution < 1 nS
- 'Global Clock Pad' connection
- Each column of the array has a Column Clock selected from one of the 8 'Global Clock' buses

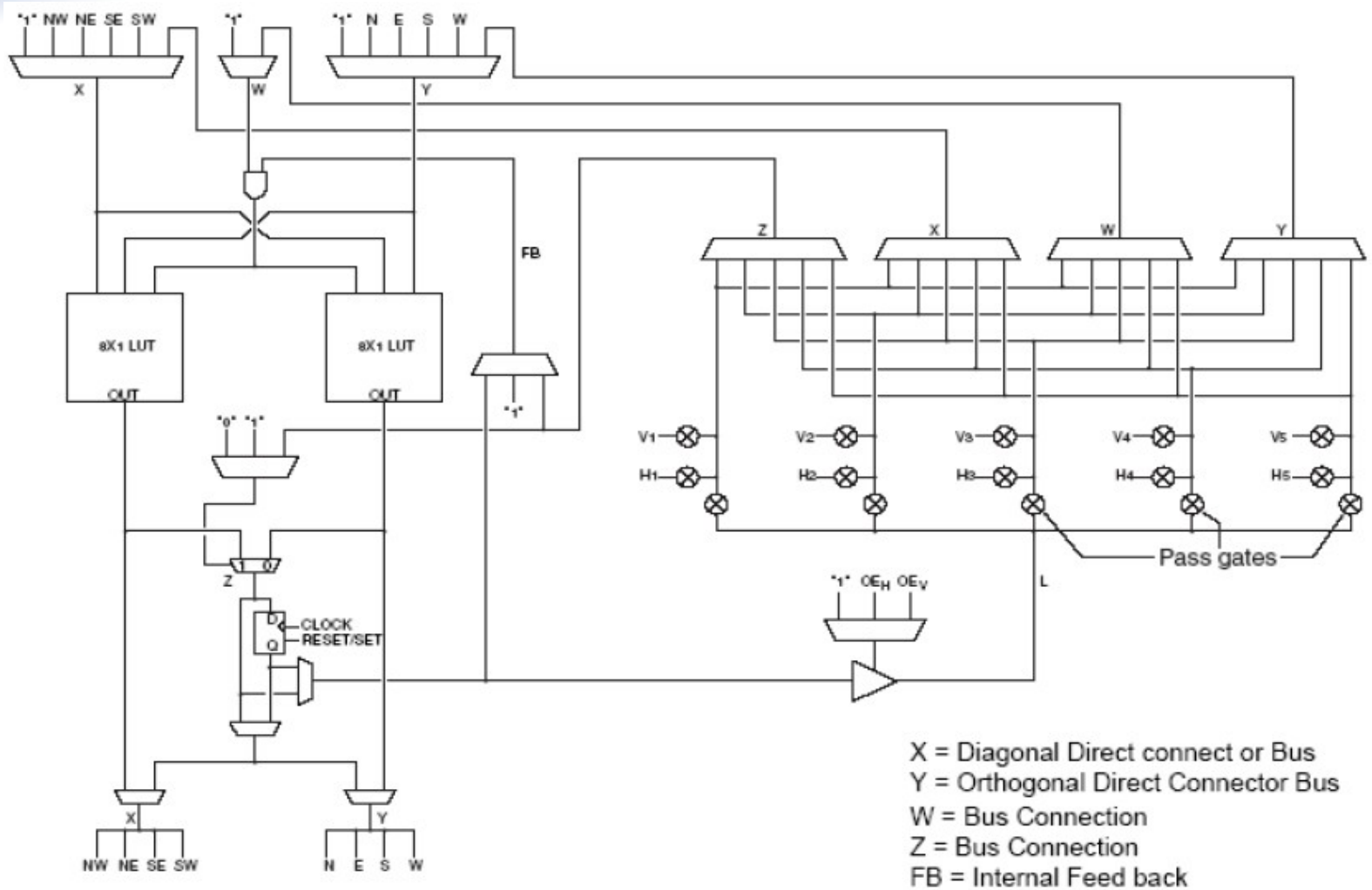
4 Additional 'Fast Clock buses'

- Only for the right/left most columns of the array
- FCK1-2 to left-side I/O
- FCK3-4 to right-side I/O

Each sector column can be clocked by

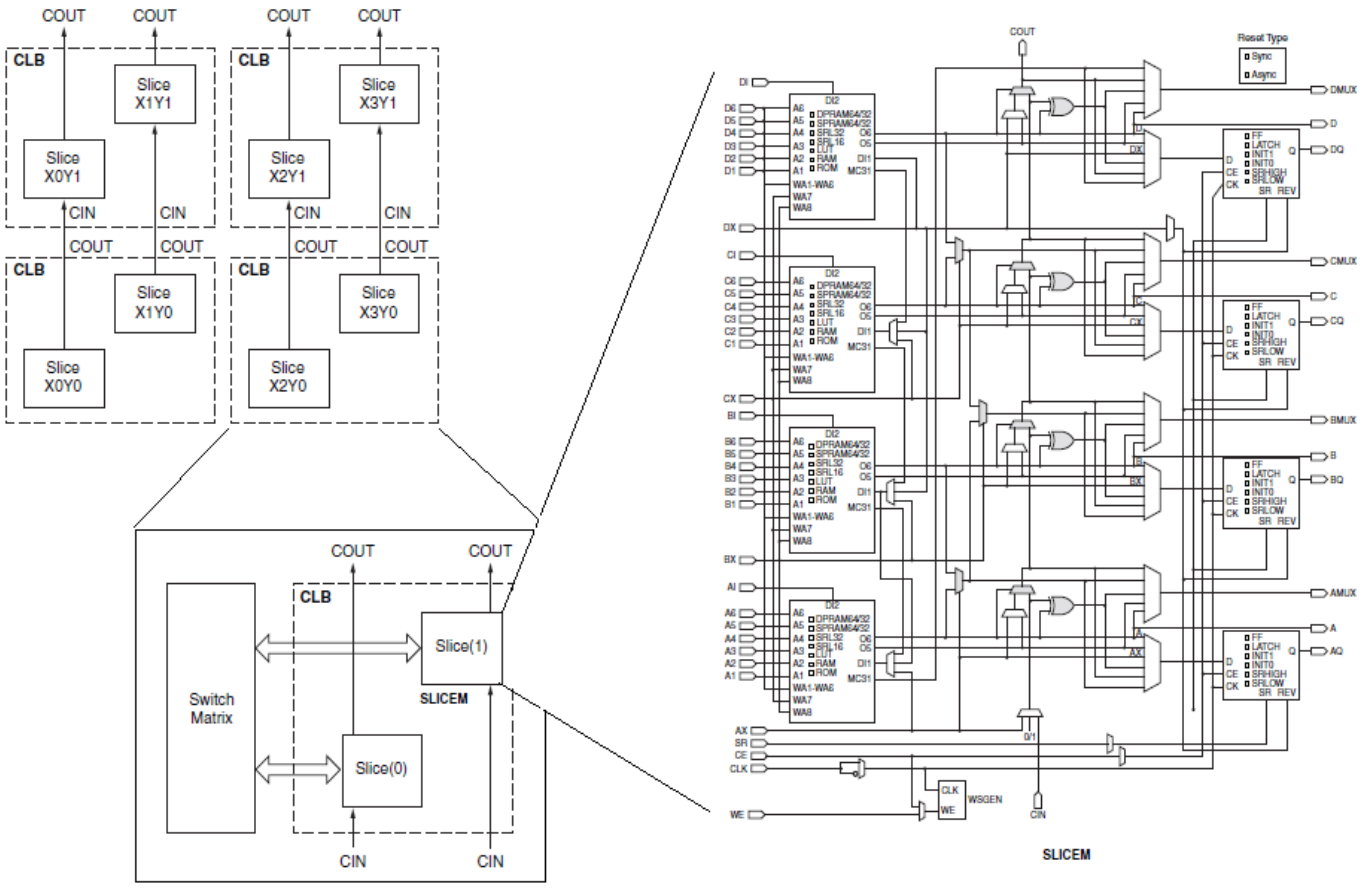
- Plane 4 'Express bus'
- Global Clock column

The ATF280E Core Cell



Virtex-5 from Xilinx : Architecture

Virtex-5 = generic logic blocks + dedicated hard IP “



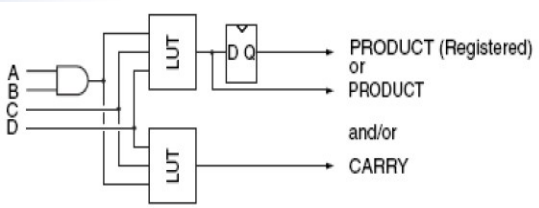
Virtex-5 "CLB" = two Slices

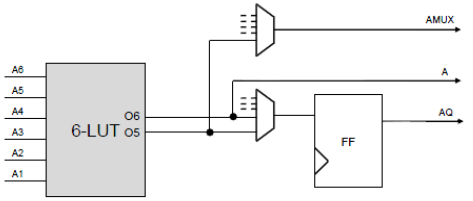
Xilinx logic block : the "Slice"

Add-on Slides

Comparison ATF280E / Virtex-5 FX130T

Equivalent elementary logic cells





1 ATF280E Core Cell ≈ ¼ of a Virtex-5 Slice

Contents of the FPGA :

14 400 Core Cells
(2 LUT + 1 FF)

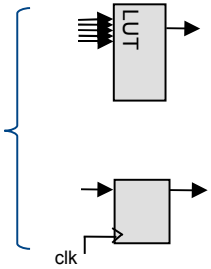
20 480 Slices
(4 LUT + 4 FF)

28 800 LUTs 3 entrées
in front of **14 400 Flip – Flops**

81 920 6-intput LUTs
in front of **81 920 Flip - Flops**

Ratios :

$$r = \frac{\text{Virtex-5}}{\text{ATF280E}}$$



Quantity of LUT inputs **r = 8,53**

Quantity of LUT memory **r = 22,8**

Flip-Flop number **r = 5,58**

Add-on Slides

SIRF Radiation Goals (src : MAPLD 2005)

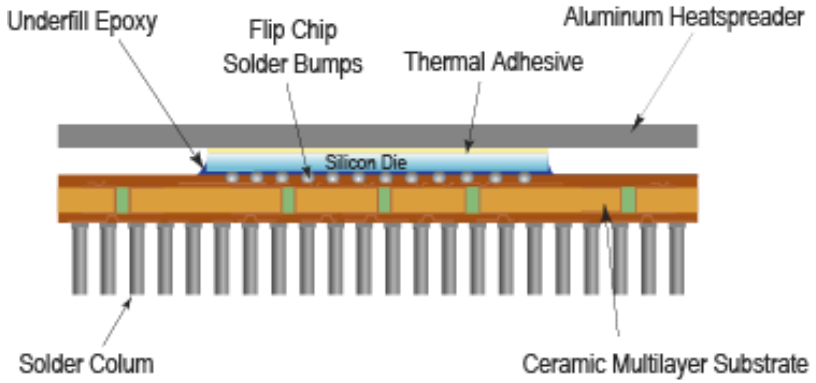
Total Dose		> 300 krad(Si) (requirement) > 1 Mrad(Si) (goal)
Dose Rate		
	Latch up	> 1×10^{10} rad(Si)/sec
	Upset	> 1×10^{9} rad(Si)/sec (requirement) > 5×10^{9} rad(Si)/sec (goal)
SEE		
	Latch up	none up to LET > 100 MeV-cm^2/mg
	Upset	threshold LET > 40 MeV-cm^2/mg, error rate < 1×10^{-10} errors/bit-day (requirement) threshold LET > 100 MeV-cm^2/mg, error rate < 1×10^{-10} errors/bit-day (goal)
	Functional Interrupt	threshold LET > 40 MeV-cm^2/mg, error rate < 1×10^{-10} errors/bit-day (requirement) threshold LET > 100 MeV-cm^2/mg, error rate < 1×10^{-10} errors/bit-day (goal)

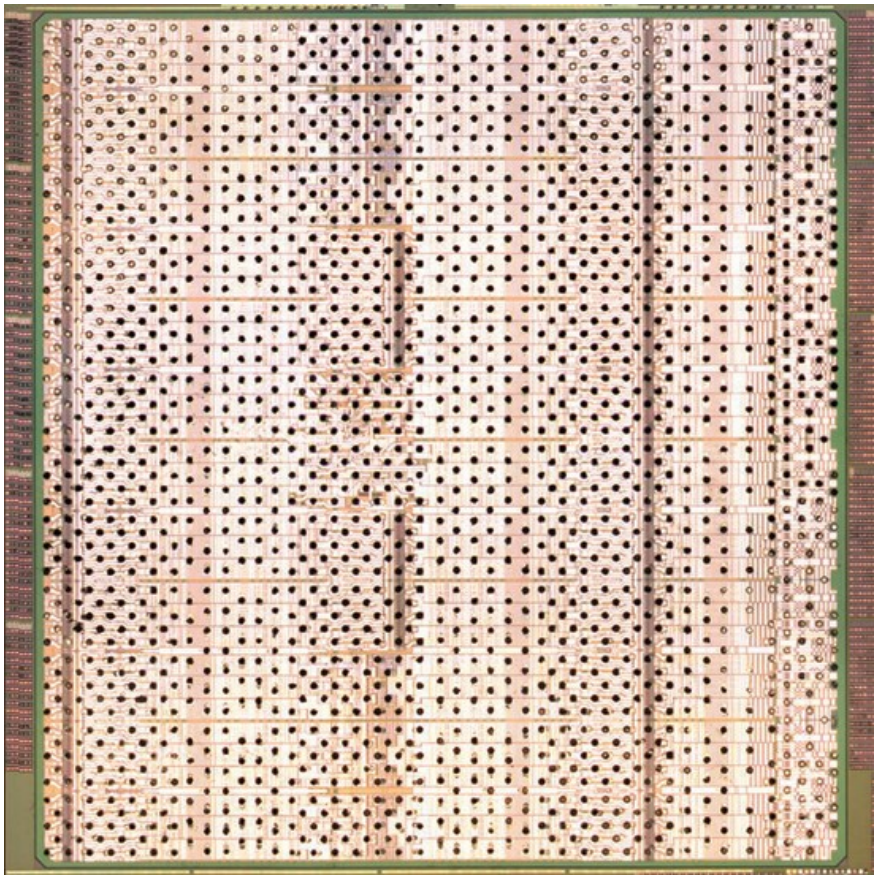
SIRF Virtex-5 packaging

Add-on Slides

SIRF : CF1144 (35x35 mm, high lead balls, MSL1)

→ Pitch :	1.00 mm
→ Solders balls :	0.60 mm Φ
→ maximun I/O :	960
- User I/Os	- 840
- Differential I/O Pairs	- 420
→ Die size :	146 mm^2
→ Die Thickness :	?



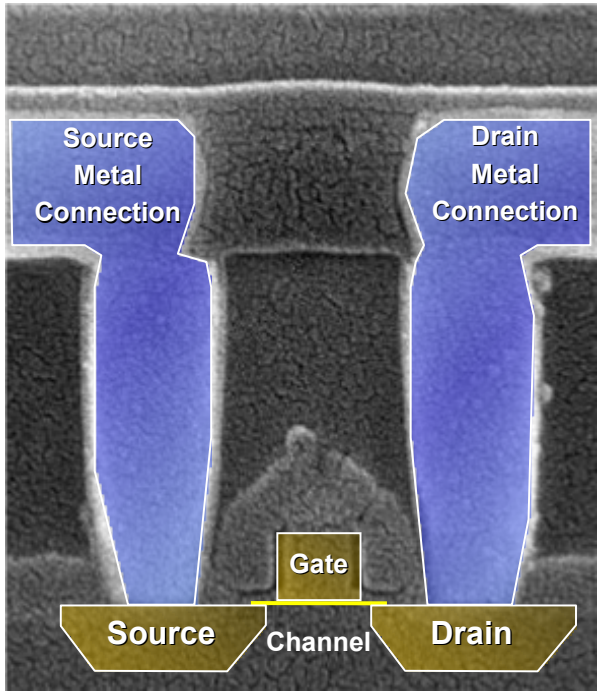


“Pictures for pleasure” : Advanced 90-nm process (Virtex-4)

Add-on Slides

Src : Xilinx

- 11-Layer metallization
10 copper + 1 aluminum
- New Triple-Oxide Structures
Lower quiescent power consumption



Virtex(220nm)
Virtex-E (180nm)
Virtex-II (150nm)
Virtex-IIpro(130nm)
XPLA3 (350nm)
CoolRunner-II (180nm)
Virtex-4 (90nm)
Spartan-3 (90nm)
Spartan-3E/3A (90nm)
Virtex-5 (65nm)